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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/415,384	03/08/2012	Francois Hebert	125.288US02	5259

94108 7590 04/11/2016
Fogg & Powers LLC/Intersil Americas LLC
4600 W 77th Street
Suite 305
Minneapolis, MN 55435

EXAMINER
WILSON, SCOTT R

ART UNIT	PAPER NUMBER
2826	

NOTIFICATION DATE	DELIVERY MODE
04/11/2016	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketing@fogglaw.com

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
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In re Patent No. 9,209,173 :
Hebert : DIRECTOR'S DECISION ON
Issue Date: December 8, 2015 : PATENT TERM ADJUSTMENT
Application No. 13/415,384 :
Filed: March 8, 2012 :
Attorney Docket No. 125.288US02 :
Title: SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD :

This is a response to the "Request for Reconsideration of Patent Term Adjustment" filed pursuant to 37 CFR 1.705(b) on February 11, 2016 requesting that the Office adjust the PTA from 181 days to 307 days.

The request for patent term adjustment is **DENIED** with respect to making any change in the patent term adjustment determination under 35 U.S.C. § 154(b) of 181 days.

THERE WILL BE NO FURTHER CONSIDERATION OF THIS MATTER BY THE OFFICE.

This decision is the Director's decision on the applicant's request for reconsideration for purposes of seeking judicial review under 35 U.S.C. § 154(b)(4).

Relevant Procedural History

On December 8, 2015, this patent issued with a patent term adjustment determination of 181 days. On February 11, 2016, patentee filed this request for redetermination of patent term adjustment with a one month extension of time, requesting that patentee be granted a patent term adjustment of 307 days.

Decision

Patentee agrees with the Office's calculation of A delay of 181 days, C delay of 0 day, 0 days of overlap and 0 days of applicant delay. Patentee disputes B delay calculated as 0 days.

Patentee contends that the USPTO failed to properly account for the delay under 35 U.S.C. §154(b)(1)(B), referred to as the "B delay." Patentee maintains that the B delay is 126 days (not 0 days). Patentee argues the time consumed by continued examination after a Request for Continued Examination does not include the time after a Notice of Allowance is mailed. With a B delay of 126, Patentee states that the correct PTA is 307 days.

The Federal Circuit reviewed the statutory interpretation of 35 U.S.C. § 154(b)(1)(B)(i) and issued a decision regarding the effects of a Request for Continued Examination ("RCE") on "B" delay in *Novartis AG v. Lee*, 740 F.3d 593 (Fed. Cir. 2014. In Novartis, the Federal Circuit agreed with the Office that "no ["B" delay] adjustment time is available for any time in continued examination, even if the continued examination was initiated more than three calendar years after the application's filing." Novartis, 740 F.3d at 601. However, the Novartis court found that if the Office issues a notice of allowance after an RCE is filed, the period after the notice of allowance should not be excluded from the "B" delay period but should be counted as "B" delay. Id. at 602.

The B delay is calculated as follows: the application was filed on March 8, 2012 and the patent issued on December 8, 2015. Thus, the application was pending for 1371 days. During this period, applicant filed one RCE on March 4, 2014. The Office mailed one Notice of Allowance, on August 4, 2015. Under 35 USC 154(b)(1)(B)(i), the time period consumed by continued examination ("RCE period") began on March 4, 2014 and ended on August 4, 2015 i.e., 519 days. Subtracting the RCE period from the total number of days the application was pending results in 1371 - 519 = 852 days. Thus, for purposes of "B" delay, the application was pending for 852 - 1096 [i.e., 3 years from the actual filing date] = 0 days beyond the three-year anniversary of the filing date.

Overall PTA Calculation

Formula:

"A" delay + "B" delay + "C" delay - Overlap - applicant delay = X

USPTO's Calculation:

181 + 0 + 0 – 0 – 0 = 181

Patentee's Calculation

181 + 126 + 0 - 0 – 0 = 307

Conclusion

Patentee remains entitled to PTA of one hundred eighty-one (181) days. Using the formula "A" delay + "B" delay + "C" delay - overlap - applicant delay = X, the amount of PTA is calculated as follows: 181 + 0 + 0 – 0 – 0 = 181 days.

Telephone inquiries specific to this matter should be directed to Attorney Advisor Charlema Grant at (571) 272-3215.

/ROBERT CLARKE/
Patent Attorney
Office of the Deputy Commissioner
for Patent Examination Policy

Office of Petitions: Routing Sheet

4700

Application No. 13415384

This application is being forwarded to your office for further processing. A decision has been rendered on a petition filed in this application, as indicated below. For details of this decision, please see the document PET.OP.DEC filed on the same date as this document.

☐ **GRANTED**

☐ **DISMISSED**

☒ **DENIED**

Office of Petitions: Decision Count Sheet

Mailing Month

Application No. 13415384

* 1 3 4 1 5 3 8 4 *

For US serial numbers: enter number only, no slashes or commas. Ex: 10123456
For PCT: enter "51+single digit of year of filing+last 5 numbers", Ex. for PCT/US05/12345, enter 51512345

Deciding Official: GRANT, CHARLEMA

Count (1) - Palm Credit 13/415,384

Decision: DENIED

FINANCE WORK NEEDED
☐ Select Check Box for YES

* D E N I E D *

Decision Type: 551 - 37 CFR 1.705(d) - PATENT TERM ADJUSTMENT AF

* 5 5 1 *

Notes:

Count (2)

Decision: n/a

FINANCE WORK NEEDED
☐ Select Check Box for YES

Decision Type: NONE

Notes:

Count (3)

Decision: n/a

FINANCE WORK NEEDED
☐ Select Check Box for YES

Decision Type: NONE

Notes:

Initials of Approving Official (if required)

If more than 3 decisions, attach 2nd count sheet & mark this box ☐

Printed on: *3/20/2016*

Patentee	Hebert
Serial No.	13/415,384
Filing Date	03/08/2012
Group Art Unit	2826
Examiner Name	Scott R. Wilson
Confirmation No.	5259
Attorney Docket No.	SE-2603-TD/125.288US02

REQUEST FOR RECONSIDERATION OF PATENT TERM ADJUSTMENT (PTA) UNDER 37 C.F.R. § 1.705(b)

Title: SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

The Patentee, under 37 C.F.R. § 1.705(b), hereby requests reconsideration of the Patent Term Adjustment (PTA) set forth in the Issue Notification dated November 18, 2015 ("Issue Notification") and also on the face of the issued U.S. Patent No. 9,209,173 ("Issued Patent"). This request for reconsideration of the PTA is accompanied by the $200 fee set forth in 37 C.F.R. § 1.18(e).

This request for reconsideration is also accompanied by a petition with the appropriate fee, to obtain a one-month extension of the period for responding to the PTA calculation, thereby moving the deadline for response from February 8, 2016 to March 8, 2016.

If necessary, please charge any additional fees or credit overpayments to Deposit Account No. 502432.

Statement of Facts

The Determination of Patent Term Adjustment included with the Issue Notification (and on face of the Issued Patent) indicated that the PTA was calculated to be 181 days. According to the USPTO's Patent Application Information Retrieval (PAIR) system, this calculation includes 181 days of "A Delays" (see 35 U.S.C. 154(b)(1)(B)) and zero days of "B Delays" (see 35 U.S.C. 154(b)(1)(B)). While agreeing with the USPTO's calculation of 181 days of "A Delays", the Patentee respectfully disagrees with the USPTO's calculation of zero days of "B Delays". Instead, as discussed below, the Patentee's opinion is that there should be 126 days of "B Delays" added to the 181 days of "A Delays", which is a total of 307 days PTA.

Specifically, according to 35 U.S.C. 154(b)(1)(B):

> **(B) Guarantee of no more than 3-year application pendency**.—Subject to the limitations under paragraph (2), if the issue of an original patent is delayed due to the failure of the United States Patent and Trademark Office to issue a patent within 3 years after the actual filing date of the application under section 111(a) in the United States or, in the case of an international application, the date of commencement of the national stage under section 371 in the international application, not including—
>
> > (i) **any time consumed by continued examination** of the application requested by the applicant under section 132(b)…

Furthermore, Chapter 2731 of the MPEP, entitled "Period of Adjustment" indicates that, based on the Federal Circuit's Novartis decision from 2014, the time consumed by continued examination after a Request for Continued Examination (RCE) does not include the time after a Notice of Allowance (NOA) is mailed. Specifically, Chapter 2731 of the MPEP states:

> The U.S. Court of Appeals for the Federal Circuit (Federal Circuit) decided that, with respect to the provisions of 35 U.S.C. 154(b)(1)(B)(i), that: (1) any time consumed by continued examination under 35 U.S.C. 132(b) is subtracted in determining the extent to which the period defined in 35 U.S.C. 154(b)(1)(B) exceeds three years, regardless of when the continued examination under 35 U.S.C. 132(b) was initiated; but (2) the **time consumed by continued examination** under 35 U.S.C. 132(b) **does not include the time after a notice of allowance is mailed**, unless the Office actually resumes examination of the application after allowance. See *Novartis AG v. Lee*, 740 F.3d 593, 109 USPQ2d 1385 (Fed. Cir. 2014).

An RCE was filed in this Application on March 4, 2014. A NOA was mailed on August 4, 2015. The Issued Patent was issued on December 8, 2015. As such the

Patentee respectfully submits that the time consumed by continued examination after the RCE (which should not be included in the "B Delays" per 35 U.S.C. 154(b)(1)(B)(i)) does not include the time after the NOA was mailed on August 4, 2015 and before the Issued Patent was issued on December 8, 2015, because the USPTO did not resume examination of the application after allowance. Accordingly, the time between the NOA mailed on August 4, 2015 and the Issued Patent issued on December 8, 2015 (126 days) should be included as "B Delays". None of these "B Delays" overlap with the "A Delays". Therefore, the USPTO should have included 126 days of "B Delays" along with the 181 days of "A Delays", which is a total of 307 days PTA.

The above-identified application is not subject to a terminal disclaimer. The Applicant believes that there are no other circumstances constituting a failure to engage in reasonable efforts to conclude processing or examination of the pending application as set forth in 37 C.F.R. § 1.704. Accordingly, the Applicant respectfully requests the Examiner to reconsider the PTA calculation and correct the total PTA to 307 days.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at 952-465-0770.

Respectfully submitted,

Date: Feb. 11, 2016

/David N Fogg/
David N. Fogg
Reg. No. 35,138

Attorneys for Patentee
Fogg & Powers LLC
4600 W 77th St, Suite 305
Minneapolis, MN 55435
T – (952) 465-0770
F – (952) 465-0771

PTO/SB/22 (03-13)
Approved for use through 3/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a)

Docket Number (Optional) SE-2603-TD/125.288US02

Application Number 13/415,384

Filed 03/08/2012

For SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD

Art Unit 2826

Examiner Scott R. Wilson

This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above-identified application.

The requested extension and fee are as follows (check time period desired and enter the appropriate fee below):

	Fee	Small Entity Fee	Micro Entity Fee	
☑ One month (37 CFR 1.17(a)(1))	$200	$100	$50	$ 200
☐ Two months (37 CFR 1.17(a)(2))	$600	$300	$150	$
☐ Three months (37 CFR 1.17(a)(3))	$1,400	$700	$350	$
☐ Four months (37 CFR 1.17(a)(4))	$2,200	$1,100	$550	$
☐ Five months (37 CFR 1.17(a)(5))	$3,000	$1,500	$750	$

☐ Applicant asserts small entity status. See 37 CFR 1.27.

☐ Applicant certifies micro entity status. See 37 CFR 1.29.
Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.

☐ A check in the amount of the fee is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director has already been authorized to charge fees in this application to a Deposit Account.

☑ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 502432.

☑ Payment made via EFS-Web.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest. See 37 CFR 3.71. 37 CFR 3.73(b) statement is enclosed (Form PTO/SB/96).

☑ attorney or agent of record. Registration number 35138.

☐ attorney or agent acting under 37 CFR 1.34. Registration number ______.

/David N Fogg/
Signature

February 11, 2016
Date

David N. Fogg
Typed or printed name

952-465-0780
Telephone Number

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.

☐ * Total of ______ forms are submitted.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	13415384
Filing Date:	08-Mar-2012
Title of Invention:	SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD
First Named Inventor/Applicant Name:	Francois Hebert
Filer:	David Fogg/Emily Reller
Attorney Docket Number:	125.288US02

Filed as Large Entity

Filing Fees for **Utility under 35 USC 111(a)**

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 1 month with $0 paid	1251	1	200	200
Miscellaneous:				
		Total in USD ($)		**200**

Electronic Acknowledgement Receipt

EFS ID:	24896236
Application Number:	13415384
International Application Number:	
Confirmation Number:	5259
Title of Invention:	SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD
First Named Inventor/Applicant Name:	Francois Hebert
Customer Number:	94108
Filer:	David Fogg/Emily Reller
Filer Authorized By:	David Fogg
Attorney Docket Number:	125.288US02
Receipt Date:	11-FEB-2016
Filing Date:	08-MAR-2012
Time Stamp:	20:22:52
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$200
RAM confirmation Number	6203
Deposit Account	502432
Authorized User	FOGG, DAVID N.

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 CFR 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 CFR 1.17 (Patent application and reexamination processing fees)

Charge any Additional Fees required under 37 CFR 1.19 (Document supply fees)

Charge any Additional Fees required under 37 CFR 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Patent Term Adjustment Petition	00532942.PDF	1013701 f0fe8b7781a4797184f68af26dd59ef0e905fbc9	no	3
Warnings:					
Information:					
2	Extension of Time	00532278.PDF	186986 90d4782b57629a9e34a360240b22502f212ea2cd	no	2
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30758 5bd961f705738dbda14bd3d2340d9cbdb65af8f1	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1231445		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronic Patent Application Fee Transmittal

Application Number:	13415384
Filing Date:	08-Mar-2012
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First Named Inventor/Applicant Name:	Francois Hebert
Filer:	David Fogg/Emily Reller
Attorney Docket Number:	125.288US02

Filed as Large Entity

Filing Fees for **Utility under 35 USC 111(a)**

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Application for patent term adjustment	1455	1	200	200
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**200**

Electronic Acknowledgement Receipt

EFS ID:	24896289
Application Number:	13415384
International Application Number:	
Confirmation Number:	5259
Title of Invention:	SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD
First Named Inventor/Applicant Name:	Francois Hebert
Customer Number:	94108
Filer:	David Fogg/Emily Reller
Filer Authorized By:	David Fogg
Attorney Docket Number:	125.288US02
Receipt Date:	11-FEB-2016
Filing Date:	08-MAR-2012
Time Stamp:	20:25:51
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$200
RAM confirmation Number	6218
Deposit Account	502432
Authorized User	FOGG, DAVID N.

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

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Charge any Additional Fees required under 37 CFR 1.19 (Document supply fees)

Charge any Additional Fees required under 37 CFR 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Fee Worksheet (SB06)	fee-info.pdf	30560 e3265bf767290f83ebc239a6e106afc709c81775	no	2

Warnings:

Information:

Total Files Size (in bytes):	30560

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

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New International Application Filed with the USPTO as a Receiving Office

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/415,384	12/08/2015	9209173	125.288US02	5259

94108 7590 11/18/2015

Fogg & Powers LLC/Intersil Americas LLC
4600 W 77th Street
Suite 305
Minneapolis, MN 55435

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 181 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Francois Hebert, San Mateo, CA;

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

94108 7590 08/04/2015
Fogg & Powers LLC/Intersil Americas LLC
4600 W 77th Street
Suite 305
Minneapolis, MN 55435

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/415,384	03/08/2012	Francois Hebert	125.288US02	5259

TITLE OF INVENTION: SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	11/04/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
WILSON, SCOTT R	2826	257-334000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Fogg & Powers LLC
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Intersil Americas LLC

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Milpitas, CA

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☒ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies ______

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

☐ A check is enclosed.
☒ Payment by credit card. ~~Form PTO-2038 is attached.~~ XXXXXXXXXXXX
☒ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 502432 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

☐ Applicant asserting small entity status. See 37 CFR 1.27

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

☐ Applicant changing to regular undiscounted fee status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Aaron W. Pederson/
Date November 4, 2015
Typed or printed name Aaron W. Pederson
Registration No. 58607

Electronic Patent Application Fee Transmittal

Application Number:	13415384
Filing Date:	08-Mar-2012
Title of Invention:	SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD
First Named Inventor/Applicant Name:	Francois Hebert
Filer:	Aaron Wesley Pederson/Emily Reller
Attorney Docket Number:	125.288US02

Filed as Large Entity

Filing Fees for **Utility under 35 USC 111(a)**

Description	**Fee Code**	**Quantity**	**Amount**	**Sub-Total in USD($)**
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**960**

Electronic Acknowledgement Receipt

EFS ID:	23983018
Application Number:	13415384
International Application Number:	
Confirmation Number:	5259
Title of Invention:	SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD
First Named Inventor/Applicant Name:	Francois Hebert
Customer Number:	94108
Filer:	Aaron Wesley Pederson/Emily Reller
Filer Authorized By:	Aaron Wesley Pederson
Attorney Docket Number:	125.288US02
Receipt Date:	04-NOV-2015
Filing Date:	08-MAR-2012
Time Stamp:	12:33:50
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$960
RAM confirmation Number	8830
Deposit Account	502432
Authorized User	PEDERSON, AARON W.

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	00505105.PDF	989942 92c086d43e1bf907f948212d91a1635fe8e4e027	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30747 eaaf28fa6f00d23ea1bc745cee5b60a4ccfed9da	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1020689		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

94108 7590 08/04/2015
Fogg & Powers LLC/Intersil Americas LLC
4600 W 77th Street
Suite 305
Minneapolis, MN 55435

EXAMINER	
WILSON, SCOTT R	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 08/04/2015

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/415,384	03/08/2012	Francois Hebert	125.288US02	5259

TITLE OF INVENTION: SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	11/04/2015

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

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94108 7590 08/04/2015
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(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/415,384	03/08/2012	Francois Hebert	125.288US02	5259

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EXAMINER	ART UNIT	CLASS-SUBCLASS
WILSON, SCOTT R	2826	257-334000

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☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

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1 ____________________
2 ____________________
3 ____________________

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(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies ____________

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number ________ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

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NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature ____________________ Date ____________________

Typed or printed name ____________________ Registration No. ____________________

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/415,384	03/08/2012	Francois Hebert	125.288US02	5259

94108 7590 08/04/2015
Fogg & Powers LLC/Intersil Americas LLC
4600 W 77th Street
Suite 305
Minneapolis, MN 55435

EXAMINER
WILSON, SCOTT R

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 08/04/2015

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)

(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	**Application No.** 13/415,384	**Applicant(s)** HEBERT, FRANCOIS	
	Examiner SCOTT R. WILSON	**Art Unit** 2826	**AIA (First Inventor to File) Status** No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Response after final filed 6/23/2015*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on______.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-20*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   Certified copies:
   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE “MAILING DATE” of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as “replacement sheets”) must be submitted.
   ☐ including changes required by the attached Examiner’s Amendment / Comment or in the Office action of Paper No./Mail Date _____.
   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner’s comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/WHITNEY T MOORE/
Primary Examiner, Art Unit 2826

DETAILED ACTION

Response to Arguments

Applicant's arguments, see pages 2-9, filed 6/23/2015, with respect to Claims 1 and 12 have been fully considered and are persuasive. The rejection of claims 1, 6, 7, 11, 12 and 15-17 has been withdrawn.

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance.

As to the 35 U.S.C. 103(a) rejection of claim 1 over Kocon in view of Bhalla, performing "an unmasked blanket body implant" in the high-side transistor (30) of Kocon, Figure 2, would make the high-side transistor inoperable, since it would contaminate critical regions, such as the high-side transistor drain, which would be unmasked.

As to the 35 U.S.C. 103(a) rejection of claim 1 over Nakamura in view of Bhalla, the method limitation of "forming a portion of a gate of the high-side transistor and a portion of a gate of the low-side transistor from a single conductive structure" is separate and distinct from any subsequent formation of circuit connections to the thus-formed gates, including formation of the driver circuit (11) of Nakamura Fig. 16, which was relied upon to teach the limitation. The meaning of this limitation is to first form a single conductive structure, then to form portions of the gates of the high-side and low-side transistors *from that structure*. The limitation of portions of the gates of the high-side and low-side transistors being formed from a single conductive structure are therefore not taught by Nakamura. Also, performing “an unmasked blanket body implant” in the high-side transistor (12) of Nakamura, Figure 3, would make the high-side transistor inoperable, since it would contaminate critical regions, such as the high-side transistor drain, which would be unmasked.

As to the 35 U.S.C. 102(b) rejection of claim 12 over Kocon, the sinker trench (70) of Kocon, Figure 2, contacts only the sidewall of the heavily doped region (62), and not the “top surface of the body contact region and a side of the body contact region”, as shown, for example, where the trench-substrate-contact (152B) expressly contacts the top and side of the body contact region (90B). The contact shown in annotated Figure 6K in the prior final rejection is not within the scope of contacting *a top surface*.

As to the 35 U.S.C. 103(a) rejection of claim 12 over Nakamura in view of Bhalla, the method limitation of "forming a portion of a gate of the high-side transistor and a portion of a gate of the low-side transistor from a single conductive structure” is separate and distinct from any subsequent formation of circuit connections to the thus-formed gates, including formation of the driver circuit (11) of Nakamura Fig. 16, which was relied upon to teach the limitation. The meaning of this limitation is to first form a single conductive structure, then to form portions of the gates of the high-side and low-side transistors from that structure. The limitation of portions of the gates of the high-side and low-side transistors being formed from a single conductive structure are therefore not taught by Nakamura.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SCOTT R. WILSON whose telephone number is (571)272-1925. The examiner can normally be reached on M, W, Th and M, Th 8:30-4:30, alternate weeks..

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Davienne Monbleau can be reached on 571-272-1945. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/S. R. W./
Examiner, Art Unit 2826

/WHITNEY T MOORE/
Primary Examiner, Art Unit 2826

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BIB DATA SHEET

CONFIRMATION NO. 5259

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
13/415,384	03/08/2012 **RULE**	257	2826	125.288US02

APPLICANTS

INVENTORS
Francois Hebert, San Mateo, CA;

** **CONTINUING DATA** *************************
This application is a CON of 12/471,911 05/26/2009 PAT 8168496
which claims benefit of 61/140,610 12/23/2008
and claims benefit of 61/162,232 03/20/2009

verified - srw

** **FOREIGN APPLICATIONS** *************************

none

** **IF REQUIRED, FOREIGN FILING LICENSE GRANTED** **
03/26/2012

		STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /SCOTT R WILSON/ Examiner's Signature	☐ Met after Allowance Initials	CA	8	20	2

ADDRESS

Fogg & Powers LLC/Intersil Americas LLC
4600 W 77th Street
Suite 305
Minneapolis, MN 55435
UNITED STATES

TITLE

SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD

FILING FEE RECEIVED 1250	FEES: Authority has been given in Paper No.____________ to charge/credit DEPOSIT ACCOUNT No.____________ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other ________________ ☐ Credit

EAST Search History

EAST Search History (Prior Art)

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S3	0	"KR 1020050085461 A"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/05 13:19
S4	1	"KR 2005085461 A"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/05 13:19
S5	2	"7459750".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/05 13:20
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S14	324	ldmos with vdmos	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/06 15:14
S15	12142	257/299,213,296,288,334,327,E21.002.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/09 15:05
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S46	19	(body with blanket with implant) and ((high-side or (high adj side)) same (low-side or (low adj side)))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/25 09:55
S47	13	S46 not S45	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/25 09:55
S48	41	"11/056346"	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/25 10:02
S49	18	"11/900616"	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/25 10:04
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S54	4664	transistor same (high-side or (high adj side)) same (low-side or (low adj side))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/26 10:30
S55	96	transistor same (high-side or (high adj side)) same (low-side or (low adj side)) and (shield with gate)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/26 11:01
S56	15	transistor same (high-side or (high adj side)) same (low-side or (low adj side)) and ((shield with gate) same (high-side or (high adj side)))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/26 11:01
S57	24514	257/299,213,296,288,334,327,E21.002.ccls. 438/238,239,270,271,386,399.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2013/07/27 07:33
S58	96	transistor same (high-side or (high adj side)) same (low-side or (low adj side)) and (shield with gate)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/27 07:33
S59	20	S58 and S57	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2013/07/27 07:33
S60	1	"13/415384"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/12/16 15:24
S61	1	(body with blanket with implant) same ((high-side or (high adj side)) same (low-side or (low adj side))) and @pd>"20130724"	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/12/18 14:05

S62	3	(body with blanket with implant) and ((high-side or (high adj side)) same (low-side or (low adj side))) and @pd>"20130724"	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/12/18 14:05
S63	27072	257/299,213,296,288,334,327,E21.002.ccls. 438/238,239,270,271,386,399.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2013/12/18 14:06
S64	97	transistor same (high-side or (high adj side)) same (low-side or (low adj side)) and (shield with gate)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/12/18 14:06
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S67	6951	(ldmos or (lateral with MOS$3)) and (vdmos or ((vertical or trench) with MOS$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2014/09/17 11:00
S68	179	(ldmos or (lateral with MOS$3)) and (vdmos or ((vertical or trench) with MOS$3)) and ((common or single) with gate) and (high adj side or high-side) and (low adj side or low-side)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2014/09/17 11:02
S69	30488	257/299,213,296,288,334,327,E21.002.ccls. 438/238,239,270,271,386,399.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2014/09/17 11:03
S70	24	(ldmos or (lateral with MOS$3)) and (vdmos or ((vertical or trench) with MOS$3)) and ((common or single) with gate) and (high adj side or high-side) and (low adj side or low-side) and S69	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2014/09/17 11:03
S71	105	(ldmos or (lateral with MOS$3)) and (vdmos or ((vertical or trench) with MOS$3)) and ((common or single) with gate) and (high adj side or high-side) and (low adj side or low-side) and " DC"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2014/09/17 11:03
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S90	355	hebert.in. and francois.in.	US-PGPUB; USPAT; EPO; JPO;	OR	ON	2015/07/23 16:21

			DERWENT			
S91	16	hebert.in. and francois.in. and high-side and low-side and blanket	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2015/07/23 16:21
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EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S22	0	(voltage and converter and output and stage and semiconductor and die and high and side and ldmos and low and side and vdmos and transistor).clm.	USPAT; UPAD	OR	OFF	2011/07/30 19:47
S34	0	(voltage and converter and output and stage and semiconductor and die and high and side and ldmos and low and side and vdmos and transistor).clm.	USPAT; UPAD	OR	OFF	2011/12/13 10:52

S101	0	(semiconductor and method and forming and die and (high-side adj body adj region) and transistor and lateral and diffusion and (low-side adj body adj region) and trench-gate and portion and gate and single and conductive and structure and body and unmasked and blanket and implant).clm.	USPAT; UPAD	OR	OFF	2015/07/23 16:48

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OK TO ENTER: /S.R.W./

Applicant(s)	Hebert	**AMENDMENT AND RESPONSE UNDER 37 C.F.R. § 1.116 EXPEDITED EXAMINATION PROCEDURE**
Serial No.	13/415,384	
Filing Date	3/8/2012	
Group Art Unit	2826	
Examiner Name	Wilson, Scott	
Confirmation No.	5259	
Attorney Docket No.	125.288US02	
Title: SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD		

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

OK TO ENTER: /S.R.W./

The Final Office Action mailed on April 23, 2015 has been reviewed. Please take the following remarks into consideration.

Remarks begin on page 2 of this paper.

OK TO ENTER: /S.R.W./

Issue Classification	**Application/Control No.** 13415384	**Applicant(s)/Patent Under Reexamination** HEBERT, FRANCOIS
	Examiner SCOTT R WILSON	**Art Unit** 2826

CPC

Symbol					**Type**	**Version**
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H01L		29	/	0692	A	2013-01-01
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H01L		29	/	4175	A	2013-01-01
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H01L		2224	/	49171	A	2013-01-01
H01L		2924	/	30107	A	2013-01-01
H01L		2924	/	3025	A	2013-01-01
H01L		2924	/	13091	A	2013-01-01
H01L		2924	/	13055	A	2013-01-01
H01L		2924	/	1461	A	2013-01-01
H01L		2924	/	12032	A	2013-01-01
H01L		2924	/	1305	A	2013-01-01
H01L		2924	/	13062	A	2013-01-01

/SCOTT R WILSON/ Examiner.Art Unit 2826 (Assistant Examiner)	7/23/2015 (Date)	**Total Claims Allowed:** 20	
/WHITNEY T MOORE/ Primary Examiner.Art Unit 2826 (Primary Examiner)	07/23/2015 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 18

Issue Classification	**Application/Control No.** 13415384	**Applicant(s)/Patent Under Reexamination** HEBERT, FRANCOIS
	Examiner SCOTT R WILSON	**Art Unit** 2826

CPC Combination Sets

Symbol					Type	Set	Ranking	Version
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/SCOTT R WILSON/ Examiner.Art Unit 2826 (Assistant Examiner)	7/23/2015 (Date)	**Total Claims Allowed:** 20	
/WHITNEY T MOORE/ Primary Examiner.Art Unit 2826 (Primary Examiner)	07/23/2015 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 18

Issue Classification	**Application/Control No.** 13415384	**Applicant(s)/Patent Under Reexamination** HEBERT, FRANCOIS
	Examiner SCOTT R WILSON	**Art Unit** 2826

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**
438	270

CROSS REFERENCE(S)

CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**				
438	259				

INTERNATIONAL CLASSIFICATION

CLAIMED					**NON-CLAIMED**				
H	0	1	L	29 / 4236					

/SCOTT R WILSON/ Examiner.Art Unit 2826 (Assistant Examiner)	7/23/2015 (Date)	**Total Claims Allowed:** 20
/WHITNEY T MOORE/ Primary Examiner.Art Unit 2826 (Primary Examiner)	07/23/2015 (Date)	O.G. Print Claim(s) 1
		O.G. Print Figure 18

Issue Classification	**Application/Control No.** 13415384	**Applicant(s)/Patent Under Reexamination** HEBERT, FRANCOIS
	Examiner SCOTT R WILSON	**Art Unit** 2826

☒ **Claims renumbered in the same order as presented by applicant** ☐ **CPA** ☐ **T.D.** ☐ **R.1.47**

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
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/SCOTT R WILSON/ Examiner.Art Unit 2826 (Assistant Examiner)	7/23/2015 (Date)	**Total Claims Allowed:** 20	
/WHITNEY T MOORE/ Primary Examiner.Art Unit 2826 (Primary Examiner)	07/23/2015 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 18

Search Notes	**Application/Control No.** 13415384	**Applicant(s)/Patent Under Reexamination** HEBERT, FRANCOIS
	Examiner SCOTT R WILSON	**Art Unit** 2826

CPC- SEARCHED

Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED

Symbol	Date	Examiner

US CLASSIFICATION SEARCHED

Class	Subclass	Date	Examiner

SEARCH NOTES

Search Notes	Date	Examiner
257/299,213,296,288,334,327,E21.002.ccls. 438/238,239,270,271,386,399.ccls. and text. See search history printout	7/24/2013	srw
257/299,213,296,288,334,327,E21.002.ccls. 438/238,239,270,271,386,399.ccls. and text. See updated search history printout	12/18/2013	srw
257/299,213,296,288,334,327,E21.002.ccls. 438/238,239,270,271,386,399.ccls. and text. See updated EAST search history	9/17/2014	srw
257/299,213,296,288,334,327,E21.002.ccls. 438/238,239,270,271,386,399.ccls. H01L27/088.cpc. H01L29/41766.cpc. H02M3/04.cpc. and text. See updated search history	4/16/2015	srw
257/299,213,296,288,334,327,E21.002.ccls. 438/238,239,270,271,386,399.ccls. H01L27/088.cpc. H01L29/41766.cpc. H02M3/04.cpc. and text. See EAST search history	7/23/2015	srw

INTERFERENCE SEARCH

US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

INTERFERENCE SEARCH			
US Class/ CPC Symbol	**US Subclass / CPC Group**	**Date**	**Examiner**
	Interference search. See EAST search history	7/23/2015	srw

Applicant(s)	Hebert	**AMENDMENT AND RESPONSE UNDER 37 C.F.R. § 1.116 EXPEDITED EXAMINATION PROCEDURE**
Serial No.	13/415,384	
Filing Date	3/8/2012	
Group Art Unit	2826	
Examiner Name	Wilson, Scott	
Confirmation No.	5259	
Attorney Docket No.	125.288US02	
Title: SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD		

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

The Final Office Action mailed on April 23, 2015 has been reviewed. Please take the following remarks into consideration.

Remarks begin on page 2 of this paper.

REMARKS

The Final Office Action mailed on April 23, 2015 has been reviewed. Claims 1-20 are pending in this application.

Rejections Under 35 U.S.C. § 102

Claim 12 was rejected under pre-AIA 35 USC § 102(b) as being anticipated by Kocon, (U.S. Publication No.2006/0231904). Applicant respectfully traverses this rejection.

Claim 12 recites in pertinent part "forming a trench-substrate-contact (TSC) … such that the TSC contacts a top surface of the body contact region and a side of the body contact region". Kocon does not disclose such language.

An example TSC (152B) contacting a top surface and a side of an example body contact region (90B) is shown in Figure 19 of the present application, reproduced below.

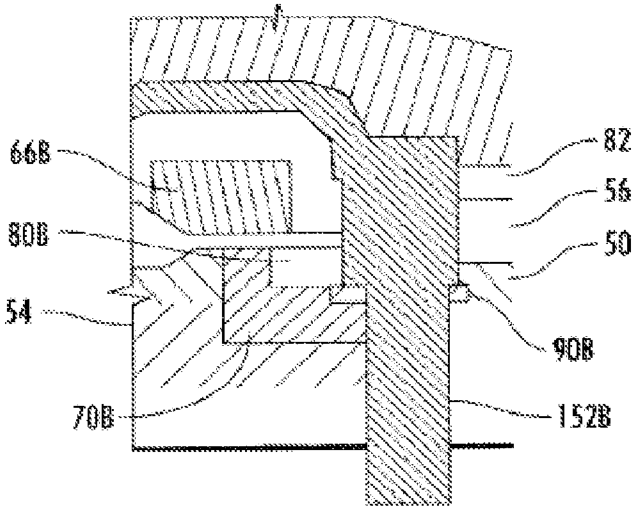

FIG. 19

On page 3, the Final Office Action dated April 23, 2015 asserted that Kocon disclosed the above language of claim 12. In particular, the Final Office Action asserted that the sinker trench (70) described in Kocon contacts a top surface and a side surface of heavily doped region 62. As asserted in Applicant's previous response, Kocon does describe that the heavily doped region 62 forms a part of a sidewall of the sinker trench (70). Kocon describes at col. 4, lines 54-58:

> Sinker trenches 70 are formed adjacent to and/or through a portion of source regions 60 and heavier-doped regions 62 of each MOSFET 36, such that the source regions 60 and heavier-doped regions 62 form at least part of the sidewalls of each sinker trench 70.

The heavily-doped region (62) forming a portion of a sidewall of the sinker trench (70) is also illustrated in Figure 2 of Kocon, reproduced below.

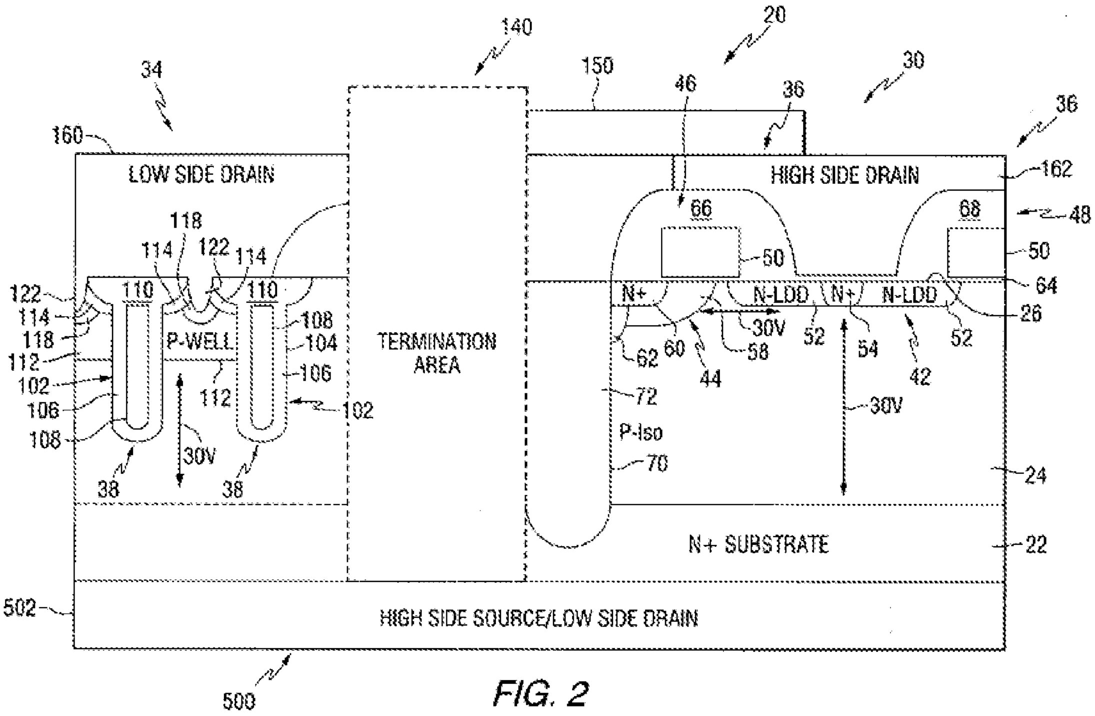

FIG. 2

Kocon, however, does not disclose that the sinker trench (70) contacts a top surface of the heavily-doped region 62. Since the sinker trench (70) disclosed in Kocon does not contact a top surface of the heavily-doped region 62, the sinker trench (70) does not correspond to the TSC of claim 12 which "contacts a top surface of the body contact region and a side of the body contact region".

For at least this reason, Applicant respectfully requests reconsideration and withdrawal of the rejection to claim 12 under pre-AIA 35 USC § 102(b) with respect to Kocon.

Rejections Under 35 U.S.C. § 103

Claim 1 was rejected under pre-AIA 35 USC § 103(a) as being unpatentable over Kocon (U.S. Publication No. 2006/0231904) in view of Bhalla et al. (U.S. Publication No. 2009/0065861). Applicant respectfully traverse this rejection.

Claim 1 recites in pertinent part:

> forming a high-side body region and a low-side body region via performing an unmasked blanket body implant performed in both a layer of the high-side transistor and a layer of the low-side transistor to form high-side and low-side body regions.

As described in paragraph [0030] of the present application:

> Advantageously, using the same body diffusion region for both the high-side region 42 and the low-side region 44 can be used because the same gate oxide and the same background doping is used for both devices. This can eliminate the need for a separate mask step to form each device and decrease other associated processing requirements, thereby reducing costs over conventional processes.

The combination of Kocon and Bhalla does not teach or suggest such language from claim 1.

The Final Office Action dated April 23, 2015 acknowledged that "Kocon does not disclose expressly forming a high-side body region and a low-side body region via an unmasked blanket body implant performed in both a layer of the high-side transistor and a layer of the low-side transistor." *Final Office Action page 7.* The Final Office Action addressed this deficiency by asserting that it would have been obvious to "form a high-side body region and a low-side body region via an unmasked blanket body implant of Bhalla in the method of formation of the power MOS device of Kocon." *Final Office Action pages 7-8.*

Applicant respectfully asserts, however, that one of ordinary skill in the art would not have formed a high-side body region and a low-side body region via an unmasked blanket body implant of Bhalla in the method of formation of the power MOS device of Kocon. In particular, using an unmasked blanket body implant in the method of formation of MOS device of Kocon, would result in body implant in undesired areas which would negatively affect the performance of the MOS devices described in Kocon.

Figure 2 of Kocon, reproduced below, illustrates an example high-side MOSFET 30 and low-side MOSFET 34 disclosed in Kocon.

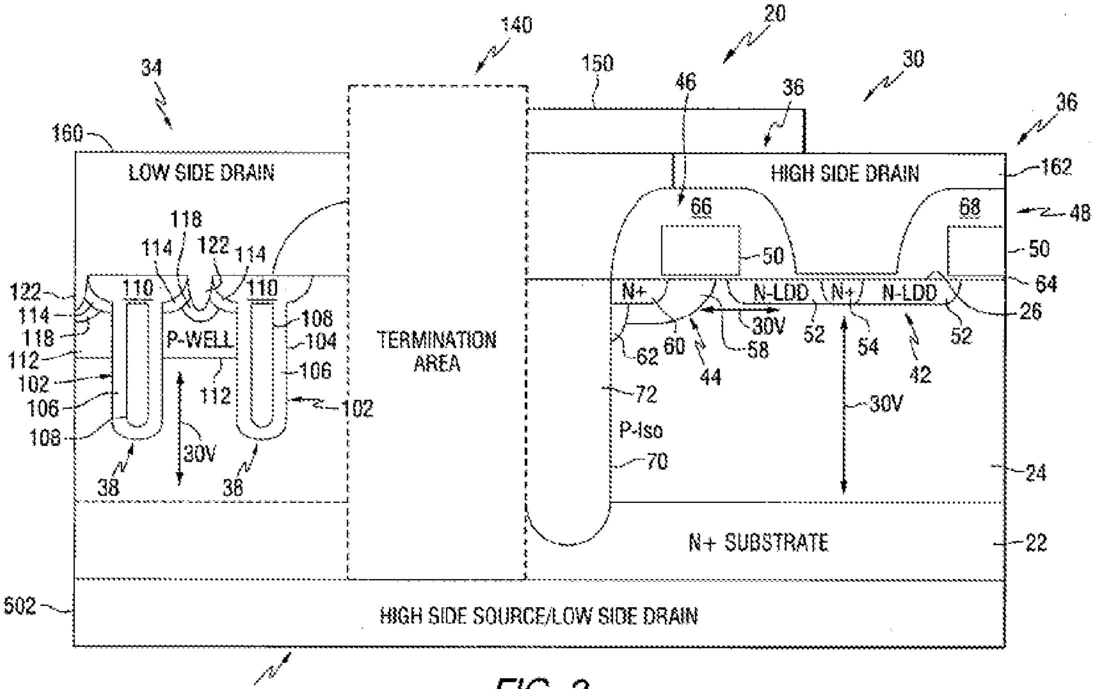

FIG. 2

As shown, the high-side MOSFET 30 disclosed in Kocon includes a drain region 52, 54, which is of a first polarity type proximate a working surface of a drift region 24. *See, Kocon at paragraph [0031] and Fig 2.* Notably, there is no body region (which is of the second polarity type – *see, paragraph [0032] of Kocon*) in or below the drain region 52, 54. Instead, the body region 58 of the high-side MOSFET 30 is formed in a limited region proximate the gate 46. *See, Kocon at paragraph [0032] and Fig. 2.* Using an unmasked blanket body implant as described in Bhalla, in the method of formation of the MOSFETs 30 and 34 of Kocon, would result in the drain region 52, 54 being doped with the second polarity type, because there would be no mask to restrict the body region dopant from the drain region. Such a second polarity type dopant in the drain region which is intended to have a first polarity type would negatively affect and likely eliminate the proper functioning of the high-side MOSFET 32 disclosed in Kocon. Accordingly, Applicant respectfully asserts that one of ordinary skill in the art would not use the unmasked blanket body implant disclosed in Bhalla in the method of formation of the MOSFETs 30 and 34 of Kocon.

For at least this reason, Applicant respectfully asserts that the combination of Bhalla and Kocon does not make obvious

> forming a high-side body region and a low-side body region via performing an unmasked blanket body implant performed in both a layer of the high-side transistor and a layer of the low-side transistor to form high-side and low-side body regions

along with the other language of claim 1. As a result, Applicant respectfully requests reconsideration and withdrawal of the rejection to claim 1 under pre-AIA 35 USC § 103(a) with respect to Kocon and Bhalla.

Claims 1, 6, 7, and 11 were rejected under pre-AIA 35 USC § 103(a) as being unpatentable over Nakamura et al. (U.S. Publication No. 2005/0179472) in view of Bhalla et al. (U.S. Publication No. 2009/0065861). Applicant respectfully traverses these rejections.

Claim 1 recites in pertinent part:

> forming a high-side body region and a low-side body region via performing an unmasked blanket body implant performed in both a layer of the high-side transistor and a layer of the low-side transistor to form high-side and low-side body regions.

As described in paragraph [0030] of the present application:

> Advantageously, using the same body diffusion region for both the high-side region 42 and the low-side region 44 can be used because the same gate oxide and the same background doping is used for both devices. This can eliminate the need for a separate mask step to form each device and decrease other associated processing requirements, thereby reducing costs over conventional processes.

The combination of Nakamura and Bhalla does not teach or suggest such language from claim 1.

Although Nakamura describes an alternative embodiment in which a low-side switching element 13 is formed on the same semiconductor substrate as a high-side switching element 12, Nakamura does not describe that the low-side switching element 13 is formed at with any of the same fabrication steps as the high-side switching element 12. Instead, Nakamura individually describes forming the low-side switching element 13 and the high-side switching element 12. *See, Nakamura at paragraphs [0088-0097].*

Bhalla, meanwhile, relates to an individual semiconductor device, and therefore, does not describe a low-side transistor on the same substrate as a high-side transistor or forming a low-side transistor with any of the same fabrication steps as used for a high-side transistor. *See, Bhalla at Abstract, Figure 1, and paragraphs [0014-0015].*

Since neither Nakamura nor Bhalla teach or suggest forming a high-side transistor using any of the same fabrication steps as a low-side transistor, it would not be obvious to one of ordinary skill in the art to perform a body implant to form both high-side and low-side body regions as recited in claim 1 based on the teachings of Nakamura and Bhalla. For at least this reason, Applicant respectfully requests reconsideration and withdrawal of the rejection to claim 1 under pre-AIA 35 USC § 103(a) with respect to Nakamura and Bhalla.

Claims 6, 7, and 11 depend from claim 1. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejections to these claims for the reasons provided above with respect to claim 1.

Claims 12 and 15-17 were rejected under pre-AIA 35 USC § 103(a) as being unpatentable over Nakamura et al. (U.S. Publication No. 2005/0179472) in view of Bhalla et al. (U.S. Publication No. 2009/0065861). Applicant respectfully traverses these rejections.

Claim 12 recites in pertinent part

> forming a single conductive structure which forms a portion of a gate of the high-side transistor and a portion of a gate of the low-side transistor from a single conductive structure;

For at least the reasons provided above with respect to claim 12, the combination of Nakamura and Bhalla does not teach or suggest the above language of claim 12. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection to claim 12 under pre-AIA 35 USC § 103(a) with respect to Nakamura and Bhalla.

Claims 15-17 depend from claim 12. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejections to these claims for the reasons provided above with respect to claim 12.

Allowable Subject Matter

Claims 2 and 3 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 4 was objected to as being dependent upon a rejected base claim, but was indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 5 was objected to as being dependent upon a rejected base claim, but was indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 8-10 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 13 and 14 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 18-20 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant thanks the Examiner for the indication of allowable subject matter.

CONCLUSION

Applicant respectfully submits that claims **1-20** are in condition for allowance and notification to that effect is earnestly requested. If necessary, please charge any additional fees or credit overpayments to Deposit Account No. 502432.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at the telephone number listed below.

Respectfully submitted,

Date: June 23, 2015

/David N Fogg/

David N. Fogg
Reg. No. 35138

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Electronic Acknowledgement Receipt

EFS ID:	22718883
Application Number:	13415384
International Application Number:	
Confirmation Number:	5259
Title of Invention:	SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD
First Named Inventor/Applicant Name:	Francois Hebert
Customer Number:	94108
Filer:	David Fogg/Emily Reller
Filer Authorized By:	David Fogg
Attorney Docket Number:	125.288US02
Receipt Date:	23-JUN-2015
Filing Date:	08-MAR-2012
Time Stamp:	19:02:00
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		00493993.PDF	1076696 d7067ebca1b66d4c3e1b5b9aaab2362b25a8ff0d	yes	10

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Response After Final Action	1	1
	Applicant Arguments/Remarks Made in an Amendment	2	10
Warnings:			
Information:			
	Total Files Size (in bytes):	1076696	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/415,384	Filing Date 03/08/2012	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	NUMBER FILED (Column 1)	NUMBER EXTRA (Column 2)	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	06/23/2015	CLAIMS REMAINING AFTER AMENDMENT (Column 1)		HIGHEST NUMBER PREVIOUSLY PAID FOR (Column 2)	PRESENT EXTRA (Column 3)	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	x $80 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	x $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	**0**

AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT (Column 1)		HIGHEST NUMBER PREVIOUSLY PAID FOR (Column 2)	PRESENT EXTRA (Column 3)	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/AJAY R. DAVID/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/415,384	03/08/2012	Francois Hebert	125.288US02	5259

94108 7590 04/23/2015
Fogg & Powers LLC/Intersil Americas LLC
4600 W 77th Street
Suite 305
Minneapolis, MN 55435

EXAMINER
WILSON, SCOTT R

ART UNIT	PAPER NUMBER
2826	

NOTIFICATION DATE	DELIVERY MODE
04/23/2015	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketing@fogglaw.com

Office Action Summary

Application No. 13/415,384	**Applicant(s)** HEBERT, FRANCOIS		
Examiner SCOTT R. WILSON	**Art Unit** 2826	**AIA (First Inventor to File) Status** No	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/19/2014*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.
3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-20* is/are pending in the application.
   5a) Of the above claim(s) _____ is/are withdrawn from consideration.
6)☐ Claim(s) _____ is/are allowed.
7)☒ Claim(s) *1,6,7,11,12 and 15-17* is/are rejected.
8)☒ Claim(s) *2-5,8-10,13,14 and 18-20* is/are objected to.
9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.
11)☒ The drawing(s) filed on *8 March 2012* is/are: a)☒ accepted or b)☐ objected to by the Examiner.
   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:
   1.☐ Certified copies of the priority documents have been received.
   2.☐ Certified copies of the priority documents have been received in Application No. _____.
   3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
   Paper No(s)/Mail Date _____.
3) ☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date. _____ .
4) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 12/19/2014 have been fully considered but they are not persuasive.

As to claim 1, in regard to the USC 103(a) rejection of Kocon in view of Bhalla, applicant argues (page 4, second para.) that “in discussing Figure 7, paragraph [0044] of Bhalla explicitly states that the blanket implant 702 is used "before the formation of the main body implant." (emphasis added). Thus, the blanket implant 702 depicted in Figure 7 is not the body implant as it is formed prior to the body implant.” Applicant argues in essence that Bhalla intends the “body region” to refer only to implanted regions bordering the upper surface of the semiconductor, such as (460a-d) of Figure 4L.

Bhalla, Figure 7, shows an optional “blanket implant” performed prior to the formation of “body regions” (460a-d). Since Bhalla teaches that (720) is a blanket implant directed at the body of the semiconductor and implanted into the body of the semiconductor, it is therefore within the scope of being a blanket body implant. In addition, Bhalla notes in [0044] that “The blanket implant *changes the body profile in the body bottom region*…” (emphasis added), implying that the blanket implant (702) can be considered a part of the body region, in the sense that “body region” is used by Bhalla. This teaching of Bhalla applies also to the USC 103(a) rejection of Nakamura in view of Bhalla.

As to claim 12, in regard to the USC 102(b) rejection over Kocon, applicant argues (page 3, upper para.) that “Nothing in Kocon teaches or suggests a TSC which "contacts a top surface of the body contact region" as claimed in claim 12. Indeed, Kocon is completely silent with respect to this limitation.”

Kocon, Figure 6E disclose formation of body contact region in the high side transistor (58)([0032], “High-side source 44 includes body well 58…”), which contacts body drift region (24)([0028]). Kocon, Figure 6H teaches subsequent doping (680) and formation of heavier doped region (62)(not labeled in Fig. 62, but indicated by context at the location shown in the annotated figure)

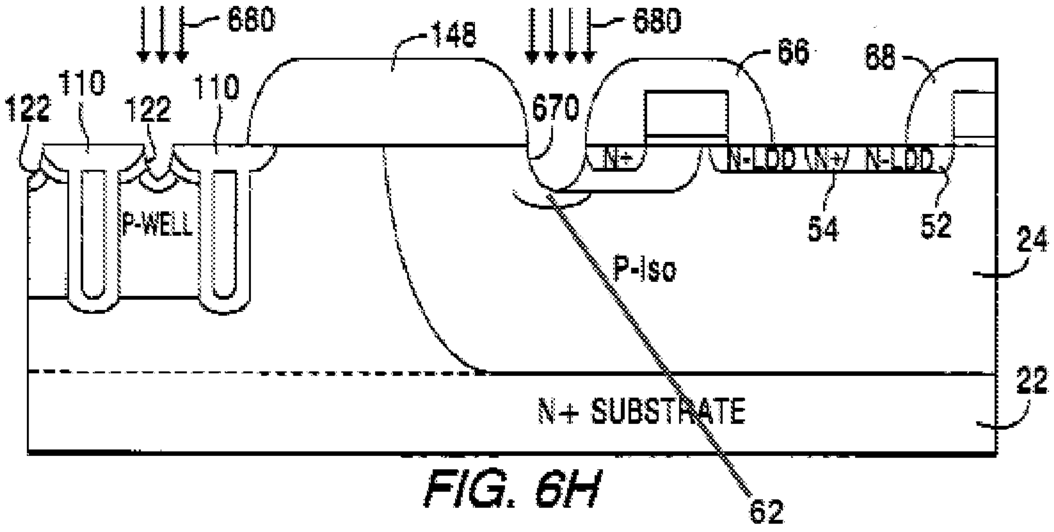

FIG. 6H

Note that the body contact region remains the body contact region, even when heavily doped. The heavily doped portion of the body contact region is shown in annotated Figure 6I, and the entire body contact region is shown in annotated Figure 6K.

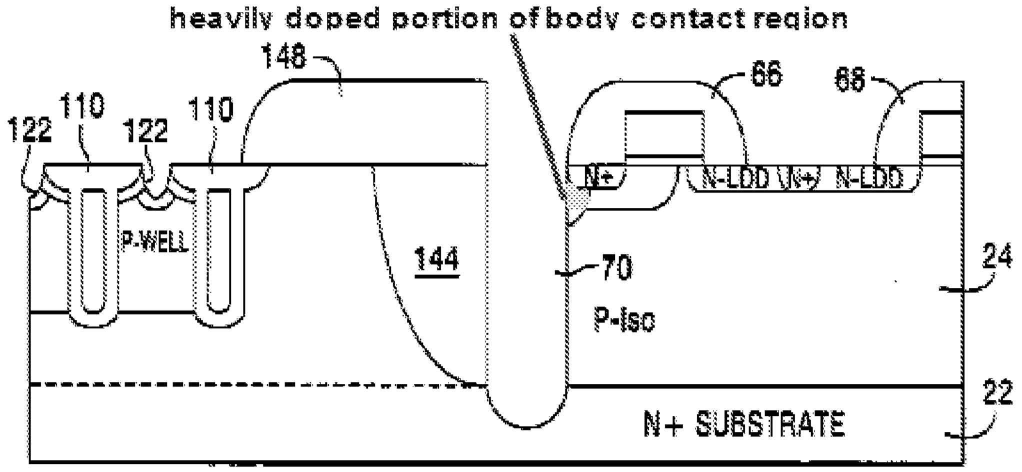

FIG. 6I

Thus, sinker trench (70), which is within the scope of being TSC (trench-substrate-contact), akin to applicants (152B) of Figure 15, contacts a top surface of the body contact region, and also a side of the body contact region.

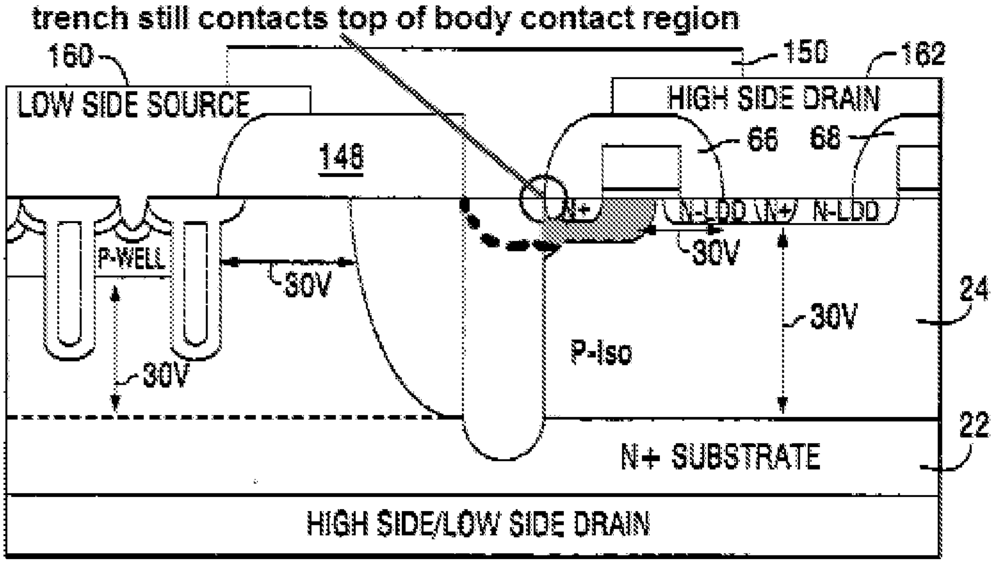

FIG. 6K

In regards to the USC 103(a) rejection of claim 12 over Nakamura in view of Bhalla, applicant argues that “Thus, the driver circuit (11) is connected to the gates, but does not form a part of the gates. Indeed, Figures 2A and 2B of Nakamura clearly show that the low side FET is not even formed on the same substrate as the driver circuit, as indicated by the dotted lines.”

The driver circuit (11) of Nakamura is a single structure, and is conductive, therefore, it is within the scope of being a single conductive structure. The driver circuit also comprises conductors which are electrically connected to the high-side and low-side gates, and which are at the same potential as the gates at all times. Thus they are within the scope of forming a portion of the high-side and low-side gates. In addition, the limitation of claim 12 does not expressly limit the portion of the gate of the high-side and low-side transistors to be on the single semiconductor die.

Claim Rejections - 35 USC § 102

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim 12 is rejected under pre-AIA 35 U.S.C. 102(b) as being anticipated by Kocon (US 2006/0231904 A1). Kocon, Figures 1 and 2, discloses a method of forming a semiconductor device, the method comprising: forming a high-side transistor (30) comprising a lateral diffusion metal oxide semiconductor (LDMOS) device on a single semiconductor die; forming a low-side transistor (34) comprising a trench-gate vertical diffusion metal oxide semiconductor (VDMOS) device on the single semiconductor die (paragraph [0029]); and forming a portion of a gate of the high-side transistor and a portion of a gate of the low-side transistor from a single conductive structure, embodied as forming high-side gate (50) and low-side gate (108) of Figure 6D from a conductive material (paragraph [0037], "Conductive material, such as, for example, highly-doped polysilicon, is disposed within the lined gate trenches 104 thereby forming gate electrodes 108").; wherein forming the high-side transistor comprises: forming a body region; forming a body contact region in the body region; and forming a trench-substrate-contact (TSC) (70) through the body contact region and the body region such that the TSC contacts a top surface of the body contact region and a side of the body contact region.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim 1 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Kocon in view of Bhalla et al. (US 2009/0065861 A1)(Bhalla). Kocon, Figures 1 and 2, discloses a method for forming a semiconductor device, the method comprising: forming, on a semiconductor die, a high-side transistor (30) comprising a lateral diffusion metal oxide semiconductor (LDMOS) device; forming, on the semiconductor die, a low-side transistor (34) comprising a trench-gate vertical diffusion metal oxide semiconductor (VDMOS) device (paragraph [0029]); and forming, on the semiconductor die, a portion of a gate of the high-side transistor and a portion of a gate of the low-side transistor from a single conductive structure, embodied as forming high-side gate (50) and low-side gate (108) of Figure 6D from a conductive material (paragraph [0037], "Conductive material, such as, for example, highly-doped polysilicon, is disposed within the lined gate trenches 104 thereby forming gate electrodes 108"). Kocon does not disclose expressly forming a high-side body region and a low-side body region via an unmasked blanket body implant performed in both a layer of the high-side transistor and a layer of the low-side transistor. Bhalla, Figure 7, discloses (paragraph [0044]) an unmasked blanket body implant that may be performed in both the high-side transistor and low-side transistor regions of a power MOS device, which may be a DC/DC converter (paragraph [0002]). At the time of invention, it would have been obvious for one of ordinary skill in the art to form a high-side body region and a low-side body region via an unmasked blanket body implant of Bhalla in the method of formation of the power MOS device of Kocon. The motivation would have been to change the body profile in the body bottom region and enhance the breakdown voltage without noticeably increasing the transistor on-resistance (Bhalla, paragraph [0044]). Therefore, it would have been obvious to combine Kocon with Bhalla to obtain the method of claim 1.

Claims 1, 6, 7 and 11 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Nakamura et al. (US 2005/0179472 A1)(Nakamura) in view of Bhalla. As to claim 1, Nakamura, Figure 16, discloses a method for forming a semiconductor device, the method comprising: forming, on a semiconductor die (paragraph [0088]), a high-side transistor (12) comprising a lateral diffusion metal oxide semiconductor (LDMOS) device (shown on the right-hand-side of Figure 3); forming, on the semiconductor die, a low-side transistor comprising a trench- gate vertical diffusion metal oxide semiconductor (VDMOS) device (paragraph [0048]-[0049] and Figure 4), and forming, on the semiconductor die, a portion of a gate of the high-side transistor and a portion of a gate of the low-side transistor from a single conductive structure, embodied as the driver circuit (11). Nakamura does not disclose expressly forming a high-side body region and a low-side body regions via an unmasked blanket body implant in a layer of the high-side transistor and a layer of the low-side transistor. Bhalla, Figure 7, discloses (paragraph [0044]) an unmasked blanket body implant that may be performed in both the high-side transistor and low-side transistor regions of a power MOS device, which may be a DC/DC converter (paragraph [0002]). At the time of invention, it would have been obvious for one of ordinary skill in the art to form a high-side body region and a low-side body region via an unmasked blanket body implant of Bhalla in the method of formation of the power MOS device of Nakamura. The motivation would have been to change the body profile in the body bottom region and enhance the breakdown voltage without noticeably increasing the transistor on-resistance (Bhalla, paragraph [0044]). Therefore, it would have been obvious to combine Nakamura with Bhalla to obtain the method of claim 1.

As to claim 6, Nakamura, Figure 2A, discloses (Abstract and paragraph [0040]) that the low side FET may be formed on a semiconductor die, which may be considered a first semiconductor die, and voltage converter controller circuitry (11) may be formed a second semiconductor die different from the first semiconductor die and that the die containing the voltage converter controller circuitry may be electrically coupled (13) with the first semiconductor die.

As to claim 7, Nakamura, Figure 2A, discloses (paragraph [0047]) co-packaging the first semiconductor die and the second semiconductor die into a single semiconductor device (2)(“package”).

As to claim 11, Nakamura, Figure 3, discloses (paragraph [0045]) forming a conductive contact within a trench to electrically couple a high-side transistor source (n^+ region 35) and a high-side transistor body (neighboring p^+ region).

Claim 12 and 15-17 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Bhalla. As to claim 12, Nakamura, Figure 16, discloses a method for forming a semiconductor device, the method comprising:

forming, on a single semiconductor die (paragraph [0088]), a high-side transistor (12) comprising a lateral diffusion metal oxide semiconductor (LDMOS) device (shown on the right-hand-side of Figure 3); forming, on the semiconductor die, a low-side transistor comprising a trench- gate vertical diffusion metal oxide semiconductor (VDMOS) device (paragraph [0048]-[0049] and Figure 4), and forming a portion of a gate of the high-side transistor and a portion of a gate of the low-side transistor from a single conductive structure, embodied as the driver circuit (11). Nakamura does not disclose expressly that forming the high-side transistor comprises: forming a body region; forming a body contact region in the body region; and forming a trench-substrate-contact (TSC) through the body contact region and the body region such that the TSC contacts a top surface of the body contact region and a side of the body contact region. Bhalla, Figure 6B, discloses an embodiment of a method of formation of a DMOS device, an example of which may be a DC-DC converter (paragraph [0026]), comprising forming a body region (N^-), forming a body contact region (Figure 4P, element 470) in the body region, and forming a trench-substrate-contact (TSC)(608) through the body contact region and the body region such that the TSC contacts a top surface of the body contact region and a side of the body contact region. At the time of invention, it would have been obvious to form the TSC of Bhalla in the method of Nakamura. The motivation would have been to form a punch-through prevention layer (Bhalla, paragraph [0042]). Therefore, it would have been obvious to combine Nakamura with Bhalla to obtain the method of claim 12.

As to claim 15, Bhalla, Figure 4U, discloses that forming the TSC comprises forming the TSC such that the TSC electrically shorts a passivation layer (480), which is within the scope of being a gate shield, for the high-side transistor to the substrate, the TSC contacting the semiconductor substrate and the body contact region on all sides of a portion of the TSC.

As to claim 16, Nakamura, Figure 2A, discloses (Abstract and paragraph [0040]) that the low side FET may be formed on a semiconductor die, which may be considered a first semiconductor die, and voltage converter controller circuitry (11) may be formed a second semiconductor die different from the first semiconductor die and that the die containing the voltage converter controller circuitry may be electrically coupled (13) with the first semiconductor die.

As to claim 17, Nakamura, Figure 2A, discloses (paragraph [0047]) co-packaging the first semiconductor die and the second semiconductor die into a single semiconductor device (2)(“package”).

Allowable Subject Matter

Claims 2 and 3 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed method which forms from a single conductive structure a shield for the high-side transistor gate, a contact to a floating guard ring, and a contact to the source of the low-side trench-gate VDMOS transistor.

Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed method which includes forming a conductive trench-source- contact structure which electrically shorts a gate shield for the high-side LDMOS transistor gate to the substrate, which contacts the semiconductor substrate, and which contacts a body contact on all sides of a portion of the trench-source-contact structure.

Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed method which forms contacts to the source and body regions of the high-side and low-side transistors, and a high-side gate shield, all from a single conductive structure.

Claims 8-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed method where a single conductive structure forms a conductive trench contact and a gate shield formed between a gate portion of the high-side LDMOS transistor and a structure overlying the gate shield.

Claims 13 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed method which forms from a single conductive structure a shield for the high-side transistor gate, a contact to a floating guard ring, and a contact to the source of the low-side trench-gate VDMOS transistor.

Claims 18-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed method where a single conductive structure forms a conductive trench contact and a gate shield formed between a gate portion of the high-side LDMOS transistor and a structure overlying the gate shield.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SCOTT R. WILSON whose telephone number is (571)272-1925. The examiner can normally be reached on M, W, Th and M, Th 8:30-4:30, alternate weeks..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Davienne Monbleau can be reached on 571-272-1945. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/S. R. W./
Examiner, Art Unit 2826

/TAN N TRAN/
Primary Examiner, Art Unit 2826

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	2	"20050179472".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/05 13:16
S2	0	"KR 20050085461 A"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/05 13:19
S3	0	"KR 1020050085461 A"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/05 13:19
S4	1	"KR 2005085461 A"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/05 13:19
S5	2	"7459750".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/05 13:20
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S7	49	("20030098468" | "20050179472" | "20050245020" | "20050280163" | "20060231904" | "20070158778" | "20070249092" | "20080023785" | "20080023825" | "20080024102" | "20090039394" | "20090057869" | "20090072368" | "20090263947" | "20100133644" | "20100140693" | "20100155837" | "20100155915" | "4924112" | "5119159" | "5242841" | "6710439" | "6812782" | "6700793").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/05 17:05
S8	5	S6 and S7	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/05 17:05
S9	136	ldmos and vdmos and (shield or cover)	US-PGPUB; USPAT; EPO; JPO;	OR	OFF	2011/04/06 13:50

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S10	58	ldmos and vdmos and ((shield or cover) with gate)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/06 13:50
S11	10	ldmos and vdmos and (((shield or cover) with gate) same ldmos)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/06 13:51
S12	1	ldmos and vdmos and (((shield or cover) with gate) same ldmos) and (guard adj ring)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/06 13:53
S13	340	ldmos same vdmos	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/06 15:14
S14	324	ldmos with vdmos	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/06 15:14
S15	12142	257/299,213,296,288,334,327,E21.002.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/09 15:05
S16	138	ldmos and vdmos and (shield or cover)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/09 15:05
S17	10	S15 and S16	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/09 15:05
S18	1	"12/320577"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/09 15:26
S19	12507	257/299,213,296,288,334,327,E21.002.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/07/30 19:43
S20	140	ldmos and vdmos and (shield or cover)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/07/30 19:43
S21	0	S19 and S20 and @pd>"20110415"	US-PGPUB; USPAT; EPO; JPO;	OR	OFF	2011/07/30 19:43

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S24	140	ldmos and vdmos and (shield or cover)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/07/30 19:54
S25	0	S23 and S24 and @pd>"20110415"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/07/30 19:54
S26	6	"12/471911"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/07/30 20:00
S27	6	("7271470" "7566931" "7618896").pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/11/05 22:13
S28	12942	257/299,213,296,288,334,327,E21.002.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/12/13 10:51
S29	150	ldmos and vdmos and (shield or cover)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/12/13 10:51
S30	1	S28 and S29 and @pd>"20110730"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/12/13 10:51
S31	20585	257/299,213,296,288,334,327,E21.002.ccls. 438/238,239,270,271,386,399.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/12/13 10:51
S32	150	ldmos and vdmos and (shield or cover)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/12/13 10:51
S33	1	S31 and S32 and @pd>"20110730"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/12/13 10:51
S36	7	(body adj implant$5) same high-side same low-side	US-PGPUB; USPAT; EPO; JPO;	OR	ON	2013/07/24 16:32

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S37	3	"4924112".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/07/24 16:45
S38	2	"6710439".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/07/24 16:46
S39	3	"6700793".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/07/24 16:52
S40	2	"20060231904".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/07/24 16:55
S41	2	"20040125573".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/07/24 17:09
S42	2	"20060231904".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/07/24 17:16
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S45	6	(body with blanket with implant) same ((high-side or (high adj side)) same (low-side or (low adj side)))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/25 09:47
S46	19	(body with blanket with implant) and ((high-side or (high adj side)) same (low-side or (low adj side)))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/25 09:55
S47	13	S46 not S45	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/25 09:55
S48	41	"11/056346"	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/25 10:02
S49	18	"11/900616"	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/25 10:04
S50	5	"12/005130"	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/25 10:07
S51	2	"20090065861".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/07/26 10:01
S52	8	(("20050245020" | "20070158778" | "20050179472" | "20080023825" | "20090039394" | "20090072368" | "20100133644" | "6812782" | "20090130799" | "20090283919" | "7732929" | "20060231904" | "20050280163" | "20100140693" | "5242841" | "7566931" | "20080203550" | "20080268577" | "6933593" | "7800208" | "20080023785" | "20080024102" | "6700793" | "20020093094" | "7042730" | "20090057869" | "20110024884" | "20030098468" | "20040262678" | "20100155837" | "7618896" | "20070034942" | "20080246086" | "6420780" | "20080017907" | "20070195563" | "6130458" | "6710439" | "7459750" | "20100155836" | "20040125573" | "20070249092" | "20090263947" | "20100155915" |	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/26 10:14

		"4924112" | "5119159" | "7271470").PN.) and (shield with gate)				
S53	1	(("20050245020" | "20070158778" | "20050179472" | "20080023825" | "20090039394" | "20090072368" | "20100133644" | "6812782" | "20090130799" | "20090283919" | "7732929" | "20060231904" | "20050280163" | "20100140693" | "5242841" | "7566931" | "20080203550" | "20080268577" | "6933593" | "7800208" | "20080023785" | "20080024102" | "6700793" | "20020093094" | "7042730" | "20090057869" | "20110024884" | "20030098468" | "20040262678" | "20100155837" | "7618896" | "20070034942" | "20080246086" | "6420780" | "20080017907" | "20070195563" | "6130458" | "6710439" | "7459750" | "20100155836" | "20040125573" | "20070249092" | "20090263947" | "20100155915" | "4924112" | "5119159" | "7271470").PN.) and (shield with gate) and (guard with ring)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/26 10:16
S54	4664	transistor same (high-side or (high adj side)) same (low-side or (low adj side))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/26 10:30
S55	96	transistor same (high-side or (high adj side)) same (low-side or (low adj side)) and (shield with gate)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/26 11:01
S56	15	transistor same (high-side or (high adj side)) same (low-side or (low adj side)) and ((shield with gate) same (high-side or (high adj side)))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/26 11:01
S57	24514	257/299,213,296,288,334,327,E21.002.ccls. 438/238,239,270,271,386,399.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2013/07/27 07:33
S58	96	transistor same (high-side or (high adj side)) same (low-side or (low adj side)) and (shield with gate)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/27 07:33
S59	20	S58 and S57	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2013/07/27 07:33
S60	1	"13/415384"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/12/16 15:24
S61	1	(body with blanket with implant) same ((high-side or (high adj side)) same (low-side or (low adj side))) and @pd>"20130724"	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/12/18 14:05

S62	3	(body with blanket with implant) and ((high-side or (high adj side)) same (low-side or (low adj side))) and @pd>"20130724"	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/12/18 14:05
S63	27072	257/299,213,296,288,334,327,E21.002.ccls. 438/238,239,270,271,386,399.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2013/12/18 14:06
S64	97	transistor same (high-side or (high adj side)) same (low-side or (low adj side)) and (shield with gate)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/12/18 14:06
S65	0	S64 and S63 and @pd>"20130724"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2013/12/18 14:06
S66	3	S61 S62	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2013/12/18 14:06
S67	6951	(ldmos or (lateral with MOS$3)) and (vdmos or ((vertical or trench) with MOS$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2014/09/17 11:00
S68	179	(ldmos or (lateral with MOS$3)) and (vdmos or ((vertical or trench) with MOS$3)) and ((common or single) with gate) and (high adj side or high-side) and (low adj side or low-side)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2014/09/17 11:02
S69	30488	257/299,213,296,288,334,327,E21.002.ccls. 438/238,239,270,271,386,399.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2014/09/17 11:03
S70	24	(ldmos or (lateral with MOS$3)) and (vdmos or ((vertical or trench) with MOS$3)) and ((common or single) with gate) and (high adj side or high-side) and (low adj side or low-side) and S69	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2014/09/17 11:03
S71	105	(ldmos or (lateral with MOS$3)) and (vdmos or ((vertical or trench) with MOS$3)) and ((common or single) with gate) and (high adj side or high-side) and (low adj side or low-side) and " DC"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2014/09/17 11:03
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S75	28	S73 S74	US-PGPUB; USPAT; EPO; JPO	OR	OFF	2014/09/17 11:36
S76	2	"20060231904".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2015/04/15 14:12
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S79	28	S77 S78	US-PGPUB; USPAT; EPO; JPO	OR	OFF	2015/04/17 20:02
S80	1	"13/415384"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2015/04/17 20:03
S81	39181	257/299,213,296,288,334,327,E21.002.ccls. 438/238,239,270,271,386,399.ccls. H01L27/088.cpc. H01L29/41766.cpc. H02M3/04.cpc.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2015/04/17 20:11
S82	66	(ldmos or (lateral with MOS$3)) and (vdmos or ((vertical or trench) with MOS$3)) and ((common or single) with gate) and (high adj side or high-side) and (low adj side or low-side) and " DC" and S81	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2015/04/17 20:11
S83	334	transistor same (high-side or (high adj side)) same (low-side or (low adj side)) and S81	US-PGPUB; USPAT; EPO; JPO	OR	ON	2015/04/17 20:12

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S22	0	(voltage and converter and output and stage and semiconductor and die and high and side and ldmos and low and side and vdmos and transistor).clm.	USPAT; UPAD	OR	OFF	2011/07/30 19:47
S34	0	(voltage and converter and output and stage and semiconductor and die and high and side and ldmos and low and side and vdmos and transistor).clm.	USPAT; UPAD	OR	OFF	2011/12/13 10:52

4/17/2015 8:13:21 PM
C:\Users\swilson3\Documents\EAST\Workspaces\13-415384 - DC-DC Converter CON.wsp

Search Notes	Application/Control No. 13415384	Applicant(s)/Patent Under Reexamination HEBERT, FRANCOIS
	Examiner SCOTT R WILSON	Art Unit 2826

CPC- SEARCHED

Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED

Symbol	Date	Examiner

US CLASSIFICATION SEARCHED

Class	Subclass	Date	Examiner

SEARCH NOTES

Search Notes	Date	Examiner
257/299,213,296,288,334,327,E21.002.ccls. 438/238,239,270,271,386,399.ccls. and text. See search history printout	7/24/2013	srw
257/299,213,296,288,334,327,E21.002.ccls. 438/238,239,270,271,386,399.ccls. and text. See updated search history printout	12/18/2013	srw
257/299,213,296,288,334,327,E21.002.ccls. 438/238,239,270,271,386,399.ccls. and text. See updated EAST search history	9/17/2014	srw
257/299,213,296,288,334,327,E21.002.ccls. 438/238,239,270,271,386,399.ccls. H01L27/088.cpc. H01L29/41766.cpc. H02M3/04.cpc. and text. See updated search history	4/16/2015	srw

INTERFERENCE SEARCH

US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

Applicant(s)	Hebert	**AMENDMENT AND RESPONSE UNDER 37 C.F.R. § 1.111**
Serial No.	13/415,384	
Filing Date	3/8/2012	
Confirmation No.	5259	
Examiner Name	WILSON, SCOTT R.	
Group Art Unit	2826	
Attorney Docket No.	125.288US02	
Title: SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD		

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

The Office Action mailed on September 29, 2014 has been reviewed. Please amend the above-identified application as follows.

Remarks begin on page 2 of this paper.

REMARKS

The Office Action mailed on September 29, 2014 has been reviewed. Claims 1-20 are pending in this application.

Rejections Under 35 U.S.C. § 102

Claim 12 was rejected under pre-AIA 35 USC § 102(b) as being anticipated by Kocon (U.S. Publication No. 2006/0231904). Applicant respectfully traverses this rejection.

Claim 12 recites:

> A method of forming a semiconductor device, the method comprising:
> forming a high-side transistor comprising a lateral diffusion metal oxide semiconductor (LDMOS) device on a single semiconductor die;
> forming a low-side transistor comprising a trench-gate vertical diffusion metal oxide semiconductor (VDMOS) device on the single semiconductor die; and
> forming a portion of a gate of the high-side transistor and a portion of a gate of the low-side transistor from a single conductive structure;
> wherein forming the high-side transistor comprises:
> forming a body region;
> forming a body contact region in the body region; and
> forming a trench-substrate-contact (TSC) through the body contact region and the body region such that the TSC contacts a top surface of the body contact region and a side of the body contact region.

Nothing in Kocon teaches or suggests all the limitations of claim 12. For example, nothing in Kocon teaches or suggests "forming a trench-substrate-contact (TSC) through the body contact region and the body region such that the TSC ***contacts a top surface of the body contact region*** and a side of the body contact region." In rejecting this limitation, the office action relies on sinker trench 70 of Kocon. However, with respect to the sinker trench 70, Kocon states "Sinker trenches 70 are formed ***adjacent to*** and/or through a portion of source regions 60 and heavier-doped regions 62 of each MOSFET 36, such that source regions 60 and heavier doped regions 62 form at least part of ***the sidewalls*** of each sinker trench 70." Col. 4 lines 54-58 (emphasis added). Thus, Kocon explicitly states that the source region 60 and heavier-doped region 62 are in contact with and form part of the sidewall of trench 70. Nothing in Kocon teaches or suggests a TSC which "contacts a top surface of the body contact region" as claimed in claim 12. Indeed, Kocon is completely silent with respect to this limitation. Therefore, for at least the reasons stated above, claim 12 is not anticipated by Kocon.

Rejections Under 35 U.S.C. § 103

Claim 1 was rejected under pre-AIA 35 USC § 103(a) as being unpatentable over Kocon (U.S. Publication No. 2006/0231904) in view of Bhalla et al. (U.S. Publication No. 2009/0065861). Applicant respectfully traverses this rejection.

Claim 1 recites:

> A method for forming a semiconductor device, the method comprising:
>
> forming, on a semiconductor die, a high-side transistor comprising a lateral diffusion metal oxide semiconductor (LDMOS) device;
>
> forming, on the semiconductor die, a low-side transistor comprising a trench-gate vertical diffusion metal oxide semiconductor (VDMOS) device;
>
> forming, on the semiconductor die, a portion of a gate of the high-side transistor and a portion of a gate of the low-side transistor from a single conductive structure; and
>
> forming a high-side body region and a low-side body region via an unmasked blanket body implant performed in both a layer of the high-side transistor and a layer of the low-side transistor.

Nothing in Kocon or Bhalla, taken alone or in combination, teaches or suggests all the limitations of claim 1. For example, nothing in the cited references teaches or suggests "forming a high-side body region and a low-side body region via an unmasked blanket body implant performed in both a layer of the high-side transistor and a layer of the low-side transistor." The office action states that Kocon does not disclose this limitation and relies on Figure 7 of Bhalla in asserting that Bhalla discloses "an unmasked blanket body implant that may be performed in both the high-side transistor and low-side transistor regions of a power MOS device." Office Action pp. 3-4.

Applicant respectfully traverses this assertion. For example, in discussing Figure 7, paragraph [0044] of Bhalla explicitly states that the blanket implant 702 is used "***before*** the formation of the main body implant." (emphasis added). Thus, the blanket implant 702 depicted in Figure 7 is not the body implant as it is formed ***prior*** to the body implant. Additionally, paragraph [0044] states "The optional modification shown in FIG. 7 may take place … prior to applying the body block ***mask*** (FIG. 4K)." (emphasis added). Thus, the step of Figure 7 occurs prior to forming the body region. Furthermore, paragraph [0044] explicitly discusses the use of a mask to form the body regions. In addition, with respect to Figure 4K, paragraph [0033] states "FIGS. 4K-4N illustrate the formation of the source and the body. In FIG. 4K, a photoresist layer 450 is patterned on the body surface ***using a body mask***. The unmasked regions are implanted with body dopants." (emphasis added). Thus, Bhalla again explicitly discusses the use of a mask to form the body region.

Therefore, nothing in the discussion of Figure 7 or elsewhere in Bhalla teaches or suggests "forming a high-side body region and a low-side body region via **an unmasked blanket body implant** performed in both a layer of the high-side transistor and a layer of the low-side transistor." Nothing in Kocon, taken alone or in combination, cures this defect of Bhalla. Indeed, Kocon also explicitly discusses the use of masks to form the body wells. See col. 8 lines 46-49. Therefore, for at least the reasons stated above, claim 1 is not obvious over Kocon in view of Bhalla.

Claims 1, 6, 7, and 11 were rejected under pre-AIA 35 USC § 103(a) as being unpatentable over Nakamura et al. (U.S. Publication No. 2005/0179472) in view of Bhalla et al. (U.S. Publication No. 2009/0065861). Applicant respectfully traverses this rejection.

Nothing in Nakamura or Bhalla teaches or suggests all the limitations of claim 1. For example, nothing in Nakamura or Bhalla teaches or suggests "forming a high-side body region and a low-side body region via an unmasked blanket body implant performed in both a layer of the high-side transistor and a layer of the low-side transistor." In addressing this limitation, the office action relies on Figure 7 of Bhalla. As discussed above, nothing in Figure 7 or elsewhere in Bhalla teaches or suggests an unmasked blanket body implant to form high-side and low-side body regions. Nothing in Nakamura cures this defect of Bhalla. Therefore, for at least the reasons stated above, claim 1 is not obvious over Nakamura in view of Bhalla.

Claims 6, 7, and 11 depend from claim 1 and, thus, are allowable for at least the same reasons as claim 1. Since Applicant believes these dependent claims are allowable for at least the above reasons, further response to all rejections have not been put forth in this response. Applicant, however, reserves the right to address said rejections if a further response is filed.

Claims 12 and 15-17 were rejected under pre-AIA 35 USC § 103(a) as being unpatentable over Nakamura et al. (U.S. Publication No. 2005/0179472) in view of Bhalla et al. (U.S. Publication No. 2009/0065861). Applicant respectfully traverses this rejection.

Nothing in Nakamura or Bhalla, taken alone or in combination, teaches or suggests all the limitations of claim 12. For example, nothing in Nakamura or Bhalla teaches or suggests "forming a portion of a gate of the high-side transistor and a portion of a gate of the low-side transistor from a single conductive structure." The office action asserts that the driver circuit 11 of Nakamura teaches this limitation. Office Action pg. 6. Applicant respectfully traverses this assertion. For example, paragraph [0038] of Nakamura states "a driver circuit 11 is connected with a gate of a high side MOS field-effect transistor … and a gate of a low side MOS field-effect transistor." Thus, the driver circuit is connected to the gates, but does not form a part of the gates. Indeed, Figures 2A and 2B of Nakamura clearly show that the low side FET is not even formed on the same substrate as the driver circuit, as indicated by the dotted lines. See paragraphs [0040] and [0050]. Furthermore, Nakamura discusses connecting the driver circuit to the gates via wires. See, for example, paragraphs [0060] and [0065]. Thus, it is not reasonable to interpret the driver circuit of Nakamura as forming a portion of the gate of the high-side transistor and a portion of the gate of the low-side transistor. Nothing in Bhalla cures this defect of Nakamura.

Therefore, for at least the reasons stated above, claim 12 is not obvious over Nakamura in view of Bhalla. Claims 15-17 depend from claim 12 and, thus, are allowable for at least the same reasons as claim 12. Since Applicant believes these dependent claims are allowable for at least the above reasons, further response to all rejections have not been put forth in this response. Applicant, however, reserves the right to address said rejections if a further response is filed.

Allowable Subject Matter

Claims 2 and 3 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 4 was objected to as being dependent upon a rejected base claim, but was indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 5 was objected to as being dependent upon a rejected base claim, but was indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 8-10 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 13 and 14 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 18-20 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

CONCLUSION

Applicant respectfully submits that claims **1-20** are in condition for allowance and notification to that effect is earnestly requested. If necessary, please charge any additional fees or credit overpayments to Deposit Account No. 502432.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at the telephone number listed below.

Respectfully submitted,

Date: December 19, 2014

/David N Fogg/
David N. Fogg
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Electronic Acknowledgement Receipt

EFS ID:	21021856
Application Number:	13415384
International Application Number:	
Confirmation Number:	5259
Title of Invention:	SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD
First Named Inventor/Applicant Name:	Francois Hebert
Customer Number:	94108
Filer:	David Fogg/Emily Reller
Filer Authorized By:	David Fogg
Attorney Docket Number:	125.288US02
Receipt Date:	19-DEC-2014
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Application Type:	Utility under 35 USC 111(a)

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Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		00465254.PDF	141041 24c1f1b6e053d536dda7226c689797495975b0e0	yes	8

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Applicant Arguments/Remarks Made in an Amendment	2	8
Warnings:			
Information:			
	Total Files Size (in bytes):	141041	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/415,384	Filing Date 03/08/2012	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	NUMBER FILED (Column 1)	NUMBER EXTRA (Column 2)	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter “0” in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	03/04/2014	CLAIMS REMAINING AFTER AMENDMENT (Column 1)		HIGHEST NUMBER PREVIOUSLY PAID FOR (Column 2)	PRESENT EXTRA (Column 3)	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	x $80 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	x $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD’L FEE	**0**

AMENDMENT	12/19/2014	CLAIMS REMAINING AFTER AMENDMENT (Column 1)		HIGHEST NUMBER PREVIOUSLY PAID FOR (Column 2)	PRESENT EXTRA (Column 3)	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	x $80 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0	x $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD’L FEE	**0**

LIE
/AJAY R. DAVID/

* If the entry in column 1 is less than the entry in column 2, write “0” in column 3.
** If the “Highest Number Previously Paid For” IN THIS SPACE is less than 20, enter “20”.
*** If the “Highest Number Previously Paid For” IN THIS SPACE is less than 3, enter “3”.
The “Highest Number Previously Paid For” (Total or Independent) is the highest number found in the appropriate box in column 1.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/415,384	03/08/2012	Francois Hebert	125.288US02	5259

94108 7590 09/29/2014

Fogg & Powers LLC/Intersil Americas LLC
4600 W 77th Street
Suite 305
Minneapolis, MN 55435

EXAMINER	
WILSON, SCOTT R	

ART UNIT	PAPER NUMBER
2826	

NOTIFICATION DATE	DELIVERY MODE
09/29/2014	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketing@fogglaw.com

Office Action Summary

Application No. 13/415,384	**Applicant(s)** HEBERT, FRANCOIS		
Examiner SCOTT R. WILSON	**Art Unit** 2826	**AIA (First Inventor to File) Status** No	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/4/2014*.
  ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.
3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-20* is/are pending in the application.
  5a) Of the above claim(s) _____ is/are withdrawn from consideration.
6)☐ Claim(s) _____ is/are allowed.
7)☒ Claim(s) *1,6,7,11,12 and 15-17* is/are rejected.
8)☒ Claim(s) *2-5,8-10,13,14 and 18-20* is/are objected to.
9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.
11)☒ The drawing(s) filed on *8 March 2012* is/are: a)☒ accepted or b)☐ objected to by the Examiner.
  Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
  Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:
  1.☐ Certified copies of the priority documents have been received.
  2.☐ Certified copies of the priority documents have been received in Application No. _____.
  3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.
3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
4) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 12 is rejected under pre-AIA 35 U.S.C. 102(b) as being anticipated by Kocon (US 2006/0231904 A1). Kocon, Figures 1 and 2, discloses a method of forming a semiconductor device, the method comprising: forming a high-side transistor (30) comprising a lateral diffusion metal oxide semiconductor (LDMOS) device on a single semiconductor die; forming a low-side transistor (34) comprising a trench-gate vertical diffusion metal oxide semiconductor (VDMOS) device on the single semiconductor die (paragraph [0029]); and forming a portion of a gate of the high-side transistor and a portion of a gate of the low-side transistor from a single conductive structure, embodied as forming high-side gate (50) and low-side gate (108) of Figure 6D from a conductive material (paragraph [0037], “Conductive material, such as, for example, highly-doped polysilicon, is disposed within the lined gate trenches 104 thereby forming gate electrodes 108”).; wherein forming the high-side transistor comprises: forming a body region; forming a body contact region in the body region; and forming a trench-substrate-contact (TSC) (70) through the body contact region and the body region such that the TSC contacts a top surface of the body contact region and a side of the body contact region.

Claim Rejections - 35 USC § 103

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Kocon in view of Bhalla et al. (US 2009/0065861 A1)(Bhalla). Kocon, Figures 1 and 2, discloses a method for forming a semiconductor device, the method comprising: forming, on a semiconductor die, a high-side transistor (30) comprising a lateral diffusion metal oxide semiconductor (LDMOS) device; forming, on the semiconductor die, a low-side transistor (34) comprising a trench-gate vertical diffusion metal oxide semiconductor (VDMOS) device (paragraph [0029]); and forming, on the semiconductor die, a portion of a gate of the high-side transistor and a portion of a gate of the low-side transistor from a single conductive structure, embodied as forming high-side gate (50) and low-side gate (108) of Figure 6D from a conductive material (paragraph [0037], “Conductive material, such as, for example, highly-doped polysilicon, is disposed within the lined gate trenches 104 therby forming gate electrodes 108”). Kocon does not disclose expressly forming a high-side body region and a low-side body region via an unmasked blanket body implant performed in both a layer of the high-side transistor and a layer of the low-side transistor. Bhalla, Figure 7, discloses (paragraph [0044]) an unmasked blanket body implant that may be performed in both the high-side transistor and low-side transistor regions of a power MOS device, which may be a DC/DC converter (paragraph [0002]). At the time of invention, it would have been obvious for one of ordinary skill in the art to form a high-side body region and a low-side body region via an unmasked blanket body implant of Bhalla in the method of formation of the power MOS device of Kocon. The motivation would have been to change the body profile in the body bottom region and enhance the breakdown voltage without noticeably increasing the transistor on-resistance (Bhalla, paragraph [0044]). Therefore, it would have been obvious to combine Kocon with Bhalla to obtain the method of claim 1.

Claims 1, 6, 7 and 11 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Nakamura et al. (US 2005/0179472 A1)(Nakamura) in view of Bhalla. As to claim 1, Nakamura, Figure 16, discloses a method for forming a semiconductor device, the method comprising: forming, on a semiconductor die (paragraph [0088]), a high-side transistor (12) comprising a lateral diffusion metal oxide semiconductor (LDMOS) device (shown on the right-hand-side of Figure 3); forming, on the semiconductor die, a low-side transistor comprising a trench- gate vertical diffusion metal oxide semiconductor (VDMOS) device (paragraph [0048]-[0049] and Figure 4), and forming, on the semiconductor die, a portion of a gate of the high-side transistor and a portion of a gate of the low-side transistor from a single conductive structure, embodied as the driver circuit (11). Nakamura does not disclose expressly forming a high-side body region and a low-side body regions via an unmasked blanket body implant in a layer of the high-side transistor and a layer of the low-side transistor.

Bhalla, Figure 7, discloses (paragraph [0044]) an unmasked blanket body implant that may be performed in both the high-side transistor and low-side transistor regions of a power MOS device, which may be a DC/DC converter (paragraph [0002]). At the time of invention, it would have been obvious for one of ordinary skill in the art to form a high-side body region and a low-side body region via an unmasked blanket body implant of Bhalla in the method of formation of the power MOS device of Nakamura. The motivation would have been to change the body profile in the body bottom region and enhance the breakdown voltage without noticeably increasing the transistor on-resistance (Bhalla, paragraph [0044]). Therefore, it would have been obvious to combine Nakamura with Bhalla to obtain the method of claim 1.

As to claim 6, Nakamura, Figure 2A, discloses (Abstract and paragraph [0040]) that the low side FET may be formed on a semiconductor die, which may be considered a first semiconductor die, and voltage converter controller circuitry (11) may be formed a second semiconductor die different from the first semiconductor die and that the die containing the voltage converter controller circuitry may be electrically coupled (13) with the first semiconductor die.

As to claim 7, Nakamura, Figure 2A, discloses (paragraph [0047]) co-packaging the first semiconductor die and the second semiconductor die into a single semiconductor device (2)(“package”).

As to claim 11, Nakamura, Figure 3, discloses (paragraph [0045]) forming a conductive contact within a trench to electrically couple a high-side transistor source (n^+ region 35) and a high-side transistor body (neighboring p^+ region).

Claim 12 and 15-17 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Bhalla. As to claim 12, Nakamura, Figure 16, discloses a method for forming a semiconductor device, the method comprising: forming, on a single semiconductor die (paragraph [0088]), a high-side transistor (12) comprising a lateral diffusion metal oxide semiconductor (LDMOS) device (shown on the right-hand-side of Figure 3); forming, on the semiconductor die, a low-side transistor comprising a trench- gate vertical diffusion metal oxide semiconductor (VDMOS) device (paragraph [0048]-[0049] and Figure 4), and forming a portion of a gate of the high-side transistor and a portion of a gate of the low-side transistor from a single conductive structure, embodied as the driver circuit (11). Nakamura does not disclose expressly that forming the high-side transistor comprises: forming a body region; forming a body contact region in the body region; and forming a trench-substrate-contact (TSC) through the body contact region and the body region such that the TSC contacts a top surface of the body contact region and a side of the body contact region. Bhalla, Figure 6B, discloses an embodiment of a method of formation of a DMOS device, an example of which may be a DC-DC converter (paragraph [0026]), comprising forming a body region (N^-), forming a body contact region (Figure 4P, element 470) in the body region, and forming a trench-substrate-contact (TSC)(608) through the body contact region and the body region such that the TSC contacts a top surface of the body contact region and a side of the body contact region. At the time of invention, it would have been obvious to form the TSC of Bhalla in the method of Nakamura. The motivation would have been to form a punch-through prevention layer (Bhalla, paragraph [0042]). Therefore, it would have been obvious to combine Nakamura with Bhalla to obtain the method of claim 12.

As to claim 15, Bhalla, Figure 4U, discloses that forming the TSC comprises forming the TSC such that the TSC electrically shorts a passivation layer (480), which is within the scope of being a gate shield, for the high-side transistor to the substrate, the TSC contacting the semiconductor substrate and the body contact region on all sides of a portion of the TSC.

As to claim 16, Nakamura, Figure 2A, discloses (Abstract and paragraph [0040]) that the low side FET may be formed on a semiconductor die, which may be considered a first semiconductor die, and voltage converter controller circuitry (11) may be formed a second semiconductor die different from the first semiconductor die and that the die containing the voltage converter controller circuitry may be electrically coupled (13) with the first semiconductor die.

As to claim 17, Nakamura, Figure 2A, discloses (paragraph [0047]) co-packaging the first semiconductor die and the second semiconductor die into a single semiconductor device (2)(“package”).

Allowable Subject Matter

Claims 2 and 3 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed method which forms from a single conductive structure a shield for the high-side transistor gate, a contact to a floating guard ring, and a contact to the source of the low-side trench-gate VDMOS transistor.

Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed method which includes forming a conductive trench-source- contact structure which electrically shorts a gate shield for the high-side LDMOS transistor gate to the substrate, which contacts the semiconductor substrate, and which contacts a body contact on all sides of a portion of the trench-source-contact structure.

Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed method which forms contacts to the source and body regions of the high-side and low-side transistors, and a high-side gate shield, all from a single conductive structure.

Claims 8-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed method where a single conductive structure forms a conductive trench contact and a gate shield formed between a gate portion of the high-side LDMOS transistor and a structure overlying the gate shield.

Claims 13 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed method which forms from a single conductive structure a shield for the high-side transistor gate, a contact to a floating guard ring, and a contact to the source of the low-side trench-gate VDMOS transistor.

Claims 18-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed method where a single conductive structure forms a conductive trench contact and a gate shield formed between a gate portion of the high-side LDMOS transistor and a structure overlying the gate shield.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SCOTT R. WILSON whose telephone number is (571)272-1925. The examiner can normally be reached on M, W, Th and M, Th 8:30-4:30, alternate weeks..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Davienne Monbleau can be reached on 571-272-1945. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

srw

/TAN N TRAN/
Primary Examiner, Art Unit 2826

Notice of References Cited	Application/Control No. 13/415,384	Applicant(s)/Patent Under Reexamination HEBERT, FRANCOIS	
	Examiner SCOTT R. WILSON	Art Unit 2826	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2006/0231904	10-2006	Kocon, Christopher B.	257/391
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	**Application/Control No.** 13415384	**Applicant(s)/Patent Under Reexamination** HEBERT, FRANCOIS
	Examiner SCOTT R WILSON	**Art Unit** 2826

CPC- SEARCHED

Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED

Symbol	Date	Examiner

US CLASSIFICATION SEARCHED

Class	Subclass	Date	Examiner

SEARCH NOTES

Search Notes	Date	Examiner
257/299,213,296,288,334,327,E21.002.ccls. 438/238,239,270,271,386,399.ccls. and text. See search history printout	7/24/2013	srw
257/299,213,296,288,334,327,E21.002.ccls. 438/238,239,270,271,386,399.ccls. and text. See updated search history printout	12/18/2013	srw
257/299,213,296,288,334,327,E21.002.ccls. 438/238,239,270,271,386,399.ccls. and text. See updated EAST search history	9/17/2014	srw

INTERFERENCE SEARCH

US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

EAST Search History

EAST Search History (Prior Art)

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S3	0	"KR 1020050085461 A"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/05 13:19
S4	1	"KR 2005085461 A"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/05 13:19
S5	2	"7459750".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/05 13:20
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S10	58	ldmos and vdmos and ((shield or cover) with gate)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/06 13:50
S11	10	ldmos and vdmos and (((shield or cover) with gate) same ldmos)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/06 13:51
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S13	340	ldmos same vdmos	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/06 15:14
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S35	1	"13/415384"	US-PGPUB; USPAT; EPO; JPO;	OR	ON	2013/07/24 14:40

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S38	2	"6710439".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/07/24 16:46
S39	3	"6700793".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/07/24 16:52
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S41	2	"20040125573".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/07/24 17:09
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S46	19	(body with blanket with implant) and ((high-side or (high adj side)) same (low-side or (low adj side)))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/25 09:55
S47	13	S46 not S45	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/25 09:55
S48	41	"11/056346"	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/25 10:02
S49	18	"11/900616"	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/25 10:04
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S54	4664	transistor same (high-side or (high adj side)) same (low-side or (low adj side))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/26 10:30
S55	96	transistor same (high-side or (high adj side)) same (low-side or (low adj side)) and (shield with gate)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/26 11:01
S56	15	transistor same (high-side or (high adj side)) same (low-side or (low adj side)) and ((shield with gate) same (high-side or (high adj side)))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/26 11:01
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S60	1	"13/415384"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/12/16 15:24

S61	1	(body with blanket with implant) same ((high-side or (high adj side)) same (low-side or (low adj side))) and @pd>"20130724"	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/12/18 14:05
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S67	6951	(ldmos or (lateral with MOS$3)) and (vdmos or ((vertical or trench) with MOS$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2014/09/17 11:00
S68	179	(ldmos or (lateral with MOS$3)) and (vdmos or ((vertical or trench) with MOS$3)) and ((common or single) with gate) and (high adj side or high-side) and (low adj side or low-side)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2014/09/17 11:02
S69	30488	257/299,213,296,288,334,327,E21.002.ccls. 438/238,239,270,271,386,399.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2014/09/17 11:03
S70	24	(ldmos or (lateral with MOS$3)) and (vdmos or ((vertical or trench) with MOS$3)) and ((common or single) with gate) and (high adj side or high-side) and (low adj side or low-side) and S69	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2014/09/17 11:03
S71	105	(ldmos or (lateral with MOS$3)) and (vdmos or ((vertical or trench) with MOS$3)) and ((common or single) with gate) and (high adj side or high-side) and (low adj side or low-side) and " DC"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2014/09/17 11:03
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S75	28	S73 S74	US-PGPUB; USPAT; EPO; JPO	OR	OFF	2014/09/17 11:36

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
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9/ 17/ 2014 4:58:35 PM
C:\ Users\ swilson3\ Documents\ EAST\ Workspaces\ 13-415384 - DC-DC Converter CON.wsp

Doc code: RCEX
Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL (Submitted Only via EFS-Web)

Application Number	13415384	Filing Date	2012-03-08	Docket Number (if applicable)	125.288US02	Art Unit	2826
First Named Inventor	HEBERT			Examiner Name	Scott R. Wilson		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☒ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on ____________
- ☐ Other ____________

☐ Enclosed

- ☐ Amendment/Reply
- ☐ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
- ☐ Other ____________

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months ____________
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other ____________

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 502432

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature
☐ Applicant Signature

Signature of Registered U.S. Patent Practitioner			
Signature	/Jay Wahlquist/	Date (YYYY-MM-DD)	2014-03-04
Name	Jay A. Wahlquist	Registration Number	55705

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	13415384
Filing Date:	08-Mar-2012
Title of Invention:	SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD
First Named Inventor/Applicant Name:	Francois Hebert
Filer:	Jay Alan Wahlquist/Jennifer Swanson
Attorney Docket Number:	125.288US02

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Request for Continued Examination	1801	1	1200	1200
	Total in USD ($)			**1200**

Electronic Acknowledgement Receipt

EFS ID:	18359508
Application Number:	13415384
International Application Number:	
Confirmation Number:	5259
Title of Invention:	SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD
First Named Inventor/Applicant Name:	Francois Hebert
Customer Number:	94108
Filer:	Jay Alan Wahlquist/Jennifer Swanson
Filer Authorized By:	Jay Alan Wahlquist
Attorney Docket Number:	125.288US02
Receipt Date:	04-MAR-2014
Filing Date:	08-MAR-2012
Time Stamp:	16:33:17
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$1200
RAM confirmation Number	3574
Deposit Account	502432
Authorized User	FOGG, DAVID N.

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Continued Examination (RCE)	00414052.PDF	697545 30f7cc24ca4ca6275af4ab3c7d3bb15987063070	no	3

Warnings:

Information:

2	Fee Worksheet (SB06)	fee-info.pdf	30462 71a34e79d41d2f46edb5e3154e6bb35f76a978ac	no	2

Warnings:

Information:

Total Files Size (in bytes):	728007

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/415,384	Filing Date 03/08/2012	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	NUMBER FILED (Column 1)	NUMBER EXTRA (Column 2)	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	03/04/2014	CLAIMS REMAINING AFTER AMENDMENT (Column 1)		HIGHEST NUMBER PREVIOUSLY PAID FOR (Column 2)	PRESENT EXTRA (Column 3)	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	x $80 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	x $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	**0**

AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT (Column 1)		HIGHEST NUMBER PREVIOUSLY PAID FOR (Column 2)	PRESENT EXTRA (Column 3)	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/PAULA BRITTON/

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/415,384	03/08/2012	Francois Hebert	125.288US02	5259

94108 7590 02/21/2014
Fogg & Powers LLC/Intersil Americas LLC
5810 W. 78th Street
Minneapolis, MN 55439

EXAMINER	
WILSON, SCOTT R	
ART UNIT	PAPER NUMBER
2826	
NOTIFICATION DATE	DELIVERY MODE
02/21/2014	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketing@fogglaw.com

Advisory Action Before the Filing of an Appeal Brief	**Application No.** *13/415,384*	**Applicant(s)** HEBERT, FRANCOIS	
	Examiner SCOTT R. WILSON	**Art Unit** 2826	**AIA (First Inventor to File) Status** No

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 30 January 2014 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

NO NOTICE OF APPEAL FILED

1. ☒ The reply was filed after a final rejection. No Notice of Appeal has been filed. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114 if this is a utility or plant application. Note that RCEs are not permitted in design applications. The reply must be filed within one of the following time periods:

   a) ☐ The period for reply expires _____months from the mailing date of the final rejection.

   b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action; or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   c) ☐ A prior Advisory Action was mailed more than 3 months after the mailing date of the final rejection in response to a first after-final reply filed within 2 months of the mailing date of the final rejection. The current period for reply expires months from the mailing date of *the prior Advisory Action* or SIX MONTHS from the mailing date of the final rejection, whichever is earlier.

   Examiner Note: If box 1 is checked, check either box (a), (b) or (c). ONLY CHECK BOX (b) WHEN THIS ADVISORY ACTION IS THE FIRST RESPONSE TO APPLICANT'S FIRST AFTER-FINAL REPLY WHICH WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. ONLY CHECK BOX (c) IN THE LIMITED SITUATION SET FORTH UNDER BOX (c). See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) or (c) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendments filed after a final rejection, but prior to the date of filing a brief, will not be entered because

   a) ☒ They raise new issues that would require further consideration and/or search (see NOTE below);

   b) ☐ They raise the issue of new matter (see NOTE below);

   c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

   d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: *See Continuation Sheet*. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).

5. ☐ Applicant's reply has overcome the following rejection(s): _____.

6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

7. ☒ For purposes of appeal, the proposed amendment(s): (a) ☒ will not be entered, or (b) ☐ will be entered, and an explanation of how the new or amended claims would be rejected is provided below or appended.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

9. ☐ The affidavit or other evidence filed after final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).

10. ☐ The affidavit or other evidence filed after the date of filing the Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing of good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).

11. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

12. ☐ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: _____.

13. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____

14. ☐ Other: _____.

STATUS OF CLAIMS

15. The status of the claim(s) is (or will be) as follows:

Claim(s) allowed: .
Claim(s) objected to: 2-5,8-10,13,14 and 18-20.
Claim(s) rejected: 1,6,7,11,12 and 15-17.
Claim(s) withdrawn from consideration: .

/TAN N TRAN/
Primary Examiner, Art Unit 2826

Continuation of 3. NOTE: At least amended claim 1 raises new issues that will require further consideration and/or search.

DO NOT ENTER: /S.R.W./

Applicant(s)	Hebert
Serial No.	13/415,384
Filing Date	3/8/2012
Group Art Unit	2826
Examiner Name	WILSON, SCOTT R.
Confirmation No.	5259
Attorney Docket No.	125.288US02

AMENDMENT AND RESPONSE UNDER 37 C.F.R. § 1.116 EXPEDITED EXAMINATION PROCEDURE

Title: SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DO NOT ENTER: /S.R.W./

The Final Office Action mailed on December 27, 2013 has been reviewed. Please amend the above-identified application as follows. This response is being submitted with a petition for consideration under the After Final Consideration Pilot program.

DO NOT ENTER: /S.R.W./

Amendments to the Claims are reflected in the listing of claims that begins on page 2 of this paper.

Remarks begin on page 10 of this paper.

DO NOT ENTER: /S.R.W./

<table>
<tr><td>Applicant(s)</td><td>Hebert</td><td rowspan="7">AMENDMENT AND RESPONSE UNDER 37 C.F.R. § 1.116 EXPEDITED EXAMINATION PROCEDURE</td></tr>
<tr><td>Serial No.</td><td>13/415,384</td></tr>
<tr><td>Filing Date</td><td>3/8/2012</td></tr>
<tr><td>Group Art Unit</td><td>2826</td></tr>
<tr><td>Examiner Name</td><td>WILSON, SCOTT R.</td></tr>
<tr><td>Confirmation No.</td><td>5259</td></tr>
<tr><td>Attorney Docket No.</td><td>125.288US02</td></tr>
<tr><td colspan="3">Title: SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD</td></tr>
</table>

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

The Final Office Action mailed on December 27, 2013 has been reviewed. Please amend the above-identified application as follows. This response is being submitted with a petition for consideration under the After Final Consideration Pilot program.

Amendments to the Claims are reflected in the listing of claims that begins on page 2 of this paper.

Remarks begin on page 10 of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of claims:

1. (Currently Amended) A method for forming a semiconductor device, the method comprising:

forming, on a semiconductor die, a high-side transistor comprising a lateral diffusion metal oxide semiconductor (LDMOS) device;

forming, on the semiconductor die, a low-side transistor comprising a trench-gate vertical diffusion metal oxide semiconductor (VDMOS) device;

forming, on the semiconductor die, ~~a single conductive structure which forms~~ a portion of a gate of the high-side transistor and a portion of a gate of the low-side transistor from a single conductive structure; and

forming a high-side body region and a low-side body region via ~~performing~~ an unmasked blanket body implant performed in both a layer of the high-side transistor and a layer of the low-side transistor ~~to form high-side and low-side body regions~~.

2. (Original) The method of claim 1 wherein the single conductive structure is a first single conductive structure and the method further comprises:

etching a layer comprising a conductor to form a contact to the semiconductor wafer section, a shield for the portion of the gate of the high-side transistor, a contact to a floating guard ring to the trench-gate VDMOS transistor, and a contact to a source of the trench-gate VDMOS transistor from a second single conductive structure.

3. (Original) The method of claim 2, further comprising etching a layer comprising a conductor to form a drain contact to a drain of the high-side LDMOS transistor, a source contact to a source of the trench-gate low-side VDMOS transistor, a gate contact to the gate of the trench-gate low-side VDMOS device, and a gate contact to the gate of the high-side transistor from a third single conductive structure.

4. (Original) The method of claim 1, further comprising forming a conductive trench-source-contact structure which electrically shorts a gate shield for the high-side LDMOS transistor gate to the substrate, which contacts the semiconductor substrate, and which contacts a body contact on all sides of a portion of the trench-source-contact structure.

5. (Original) The method of claim 1 wherein the single conductive structure is a first single conductive structure and the method further comprises forming a second single conductive structure which forms:

a contact to a source region of the high-side transistor;

a contact to a body region of the high-side transistor;

a contact to a source region of the low-side transistor;

a contact to a body region of the low-side transistor;

a gate shield for a transistor gate of the high-side transistor;

an electrical connection between the source and body of the high-side device; and

an electrical connection between a drain of the low-side device and a semiconductor substrate of the semiconductor die.

6. (Original) The method of claim 1, wherein the semiconductor die is a first semiconductor die and the method further comprises:

providing a second semiconductor die different from the first semiconductor die comprising voltage converter controller circuitry; and

electrically coupling the voltage converter controller circuitry with the first semiconductor die.

7. (Original) The method of claim 6, further comprising co-packaging the first semiconductor die and the second semiconductor die into a single semiconductor device.

8. (Original) The method of claim 1 wherein the single conductive structure is a first single conductive structure and the method further comprises:

forming a conductive trench contact having at least a portion within a trench in a semiconductor substrate;

forming at least one conductive gate portion of the LDMOS device; and

forming a gate shield interposed between the at least one conductive gate portion of the LDMOS device and a structure which overlies the gate shield,

wherein the gate shield and the conductive trench contact are formed from a second single conductive structure.

9. (Original) The method of claim 8 further comprising etching a layer comprising a conductor to define:

a conductive drain interconnect electrically coupled to a drain of the LDMOS device; and

a conductive source interconnect electrically coupled to a source of the VDMOS device,

wherein the conductive drain interconnect and the conductive source interconnect are formed from a third single conductive structure.

10. (Original) The method of claim 9, further comprising:

electrically coupling a portion of the third single conductive structure which forms the conductive drain interconnect to voltage in (VIN); and

electrically coupling a portion of the third single conductive structure which forms the conductive source interconnect to ground.

11. (Original) The method of claim 1 further comprising forming a conductive contact within a trench to electrically couple a high-side transistor source and a high-side transistor body.

12. (Currently Amended) A method of forming a semiconductor device, the method comprising:

forming a high-side transistor comprising a lateral diffusion metal oxide semiconductor (LDMOS) device on a single semiconductor die;

forming a low-side transistor comprising a trench-gate vertical diffusion metal oxide semiconductor (VDMOS) device on the single semiconductor die; and

forming ~~a single conductive structure which forms~~ a portion of a gate of the high-side transistor and a portion of a gate of the low-side transistor <u>from a single conductive structure</u>;

wherein forming the high-side transistor comprises:

forming a body region;

forming a body contact region in the body region; and

forming a trench-substrate-contact (TSC) through the body contact region and the body region such that the TSC contacts a top surface of the body contact region and a side of the body contact region.

13. (Original) The method of claim 12 wherein the single conductive structure is a first single conductive structure and the method further comprises:

forming a second single conductive structure which forms a contact to the semiconductor wafer section, a shield for the portion of the gate of the high-side transistor, a contact to a floating guard ring to the trench-gate VDMOS transistor, and a contact to a source of the trench-gate VDMOS transistor.

14. (Original) The method of claim 13, further comprising:

forming a third single conductive structure which forms a drain contact to a drain of the high-side LDMOS transistor, a source contact to a source of the trench-gate low-side VDMOS transistor, and a gate contact to the trench-gate low-side VDMOS device gate.

15. (Original) The method of claim 12, wherein forming the TSC comprises forming the TSC such that the TSC electrically shorts a gate shield for the high-

side transistor to the substrate, the TSC contacting the semiconductor substrate and the body contact region on all sides of a portion of the TSC.

16. (Original) The method of claim 12, wherein the single semiconductor die is a first semiconductor die and the method further comprising:

forming a second semiconductor die different from the first semiconductor die comprising voltage converter controller circuitry electrically coupled with the first semiconductor die.

17. (Original) The method of claim 16, further comprising co-packaging the first semiconductor die and the second semiconductor die into a single semiconductor device.

18. (Original) The method of claim 12 wherein the single conductive structure is a first single conductive structure, and the method further comprises:

forming a conductive trench contact having at least a portion within a trench within a semiconductor substrate;

forming at least one conductive gate portion of the LDMOS device; and

forming a gate shield interposed between the at least one conductive gate portion of the LDMOS device and a structure which overlies the gate shield, wherein the gate shield and the conductive trench contact are a second single conductive structure.

19. (Original) The method of claim 18 further comprising:

forming a conductive drain interconnect electrically coupled to a drain of the LDMOS device; and

forming a conductive source interconnect electrically coupled to a source of the VDMOS device,

wherein the conductive drain interconnect and the conductive source interconnect are a third single conductive structure.

20. (Original) The method of claim 19, further comprising:

electrically coupling the conductive drain interconnect to voltage in (VIN); and

electrically coupling the conductive source interconnect to ground.

REMARKS

The Final Office Action mailed on December 27, 2013 has been reviewed. Claims 1-20 are pending in this application. Claims 1 and 12 have been amended. Support for these amendments can be found, for example, in paragraphs [0028]-[0030]. Thus, no new matter has been added through these amendments.

Rejections Under 35 U.S.C. § 103

Claims 1, 6, 7, and 11 were rejected under pre-AIA 35 USC § 103(a) as being unpatentable over Nakamura et al. (U.S. Publication No. 2005/0179472) in view of Bhalla et al. (U.S. Publication No. 2009/0065861). Applicant respectfully traverses this rejection.

Claim 1, as amended, recites:

> A method for forming a semiconductor device, the method comprising:
>
> forming, on a semiconductor die, a high-side transistor comprising a lateral diffusion metal oxide semiconductor (LDMOS) device;
>
> forming, on the semiconductor die, a low-side transistor comprising a trench-gate vertical diffusion metal oxide semiconductor (VDMOS) device;
>
> forming, on the semiconductor die, ~~a single conductive structure which forms~~ a portion of a gate of the high-side transistor and a portion of a gate of the low-side transistor from a single conductive structure; and
>
> forming a high-side body region and a low-side body region via ~~performing~~ an unmasked blanket body implant performed in both a layer of the high-side transistor and a layer of the low-side transistor ~~to form high-side and low-side body regions~~.

Claim 1 has been amended to clarify the scope of the claimed limitations by making explicit what was previously at least implicit. In particular, claim 1 has been amended to clarify that the portion of the gate of the high-side transistor and the gate of the low-side transistor are formed from a single conductive structure. This was previously recited in claim 1 as "forming, on the semiconductor die, a single conductive structure which forms a portion of a gate" of the high and low side transistors. In addressing this limitation, the Office Action relied on "horizontal and vertical lines above the interlayer insulation film layer (38)" in Fig. 3 of Nakamura. (FOA pg. 2). In particular, the Office Action asserted that "These wiring layers are within the scope of being a single conductive structure, in that they are physically touching and electrically conducting." (FOA pg. 2).

Claim 1 has been amended to make explicit that the gates of the high and low side devices are formed from a single conductive structure. Even if a wire which is in physical contact with a transistor gate can be interpreted as forming a portion of the gate, which Applicant does not concede, nothing in Fig. 3 or elsewhere of Nakamura teaches or suggests a single conductive structure from which a portion of the gate of both the high-side and the low-side devices are formed. Indeed, coupling wires to the gates does not teach or suggest forming the gates of the high and low side devices from the wiring. Additionally, even if physical contact of the wiring forms a portion of the gate in Nakamura, separate wiring is used to couple the low-side gate to the driver circuit than is used for the high-side gate. Otherwise, the low-side gate would be electrically coupled to the high-side gate and the switching operation would be impaired, as understood by one of skill in the art. Additionally, there is no teaching or suggestion in Nakamura that the wiring for the low-side device and the wiring for the high-side were formed from a single conductive structure. Thus, for at least the reasons stated above, nothing in the discussion of wiring coupled to a gate of transistors in Nakamura teaches or suggests the claimed "forming, on the semiconductor die, a portion of a gate of the high-side transistor and a portion of a gate of the low-side transistor ***from a single conductive structure***."

Furthermore, nothing in Nakamura or Bhalla teaches or suggests "forming a high-side body region and a low-side body region via an unmasked blanket body implant performed in both a layer of the high-side transistor and a layer of the low-side transistor." Thus, the amendment to claim 1 makes more explicit that the high-side body region and the low-side body region are formed by performing an unmasked blanket body implant in both the high-side device and the low-side device. However, the blanket implant in Bhalla, relied on in the Office Action, does not form a body region. For example, paragraph [0044] of Bhalla states "The blanket implant is used to adjust epi profile ***without resulting in polarity changing in the epi***" and that the blanket implant is formed "before the formation of the main body implant." Since the blanket implant does not result in a polarity change in the epi, it does not teach forming a body region in the epi. Thus, even if combined with Nakamura, the blanket implant of Bhalla relied on in the Office Action does not teach or suggest forming body regions in a high-side LDMOS and in a low-side trench-gate VDMOS by performing an unmasked blanket implant in both the LDMOS and the VDMOS.

For at least the reasons stated above, nothing in Nakamura and Bhalla, taken alone or in combination, teaches or suggests all the claimed limitations of claim 1. Claims 6, 7, and 11 depend from claim 1 and, thus, are allowable for at least the same reasons as claim 1. Since Applicant believes these dependent claims are allowable for at least the above reasons, further response to all rejections have not been put forth in this response. Applicant, however, reserves the right to address said rejections if a further response is filed.

Claims 12 and 15-17 were rejected under pre-AIA 35 USC § 103(a) as being unpatentable over Nakamura et al. (U.S. Publication No. 2005/0179472) in view of Bhalla et al. (U.S. Publication No. 2009/0065861). Applicant respectfully traverses this rejection.

<u>Claim 12, as amended, recites:</u>

> A method of forming a semiconductor device, the method comprising:
>
> forming a high-side transistor comprising a lateral diffusion metal oxide semiconductor (LDMOS) device on a single semiconductor die;

> forming a low-side transistor comprising a trench-gate vertical diffusion metal oxide semiconductor (VDMOS) device on the single semiconductor die; and
>
> forming ~~a single conductive structure which forms~~ a portion of a gate of the high-side transistor and a portion of a gate of the low-side transistor <u>from a single conductive structure</u>;
>
> wherein forming the high-side transistor comprises:
>
> forming a body region;
>
> forming a body contact region in the body region; and
>
> forming a trench-substrate-contact (TSC) through the body contact region and the body region such that the TSC contacts a top surface of the body contact region and a side of the body contact region.

Claim 12 has been amended similar to claim 1 to make more explicit that a portion of the gate of the high-side transistor and the low-side transistor are formed from a single conductive structure. As discussed above with respect to claim 1, nothing in Nakamura teaches or suggests this limitation. Nothing in Bhalla cures this defect of Nakamura. Therefore, for at least the reasons stated above, claim 12 is not obvious over Nakamura in view of Bhalla.

Claims 15-17 depend from claim 12 and, thus, are allowable for at least the reasons stated above. Since Applicant believes these dependent claims are allowable for at least the above reasons, further response to all rejections have not been put forth in this response. Applicant, however, reserves the right to address said rejections if a further response is filed.

Allowable Subject Matter

Claims 2-5, 8-10, 13-14, and 18-20 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

CONCLUSION

Applicant respectfully submits that claims **1-20** are in condition for allowance and notification to that effect is earnestly requested. If necessary, please charge any additional fees or credit overpayments to Deposit Account No. 502432.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at the telephone number listed below.

Respectfully submitted,

Date: January 29, 2014 /David N Fogg/

David N. Fogg
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REMARKS

The Final Office Action mailed on December 27, 2013 has been reviewed. Claims 1-20 are pending in this application. Claims 1 and 12 have been amended. Support for these amendments can be found, for example, in paragraphs [0028]-[0030]. Thus, no new matter has been added through these amendments.

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Claim 1, as amended, recites:

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>
> forming, on a semiconductor die, a high-side transistor comprising a lateral diffusion metal oxide semiconductor (LDMOS) device;
>
> forming, on the semiconductor die, a low-side transistor comprising a trench-gate vertical diffusion metal oxide semiconductor (VDMOS) device;
>
> forming, on the semiconductor die, ~~a single conductive structure which forms~~ a portion of a gate of the high-side transistor and a portion of a gate of the low-side transistor from a single conductive structure; and
>
> forming a high-side body region and a low-side body region via ~~performing~~ an unmasked blanket body implant performed in both a layer of the high-side transistor and a layer of the low-side transistor ~~to form high-side and low-side body regions~~.

Claim 1 has been amended to clarify the scope of the claimed limitations by making explicit what was previously at least implicit. In particular, claim 1 has been amended to clarify that the portion of the gate of the high-side transistor and the gate of the low-side transistor are formed from a single conductive structure. This was previously recited in claim 1 as "forming, on the semiconductor die, a single conductive structure which forms a portion of a gate" of the high and low side transistors. In addressing this limitation, the Office Action relied on "horizontal and vertical lines above the interlayer insulation film layer (38)" in Fig. 3 of Nakamura. (FOA pg. 2). In particular, the Office Action asserted that "These wiring layers are within the scope of being a single conductive structure, in that they are physically touching and electrically conducting." (FOA pg. 2).

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For at least the reasons stated above, nothing in Nakamura and Bhalla, taken alone or in combination, teaches or suggests all the claimed limitations of claim 1. Claims 6, 7, and 11 depend from claim 1 and, thus, are allowable for at least the same reasons as claim 1. Since Applicant believes these dependent claims are allowable for at least the above reasons, further response to all rejections have not been put forth in this response. Applicant, however, reserves the right to address said rejections if a further response is filed.

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forming ~~a single conductive structure which forms~~ a portion of a gate of the high-side transistor and a portion of a gate of the low-side transistor from a single conductive structure;

wherein forming the high-side transistor comprises:

forming a body region;

forming a body contact region in the body region; and

forming a trench-substrate-contact (TSC) through the body contact region and the body region such that the TSC contacts a top surface of the body contact region and a side of the body contact region.

Claim 12 has been amended similar to claim 1 to make more explicit that a portion of the gate of the high-side transistor and the low-side transistor are formed from a single conductive structure. As discussed above with respect to claim 1, nothing in Nakamura teaches or suggests this limitation. Nothing in Bhalla cures this defect of Nakamura. Therefore, for at least the reasons stated above, claim 12 is not obvious over Nakamura in view of Bhalla.

Claims 15-17 depend from claim 12 and, thus, are allowable for at least the reasons stated above. Since Applicant believes these dependent claims are allowable for at least the above reasons, further response to all rejections have not been put forth in this response. Applicant, however, reserves the right to address said rejections if a further response is filed.

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Claims 2-5, 8-10, 13-14, and 18-20 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

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If the Examiner has any questions or concerns regarding this application, please contact the undersigned at the telephone number listed below.

Respectfully submitted,

Date: January 29, 2014

/David N Fogg/

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Reg. No. 35138

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Minneapolis, MN 55439
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Doc Code: A.NE.AFCP
Document Description: After Final Consideration Pilot Program Request

PTO/SB/434 (05-13)

CERTIFICATION AND REQUEST FOR CONSIDERATION UNDER THE AFTER FINAL CONSIDERATION PILOT PROGRAM 2.0

Practitioner Docket No.: 125.288US02/SE-2603-TD	Application No.: 13/415,384	Filing Date: 3/8/2012
First Named Inventor: Francois Hebert	Title: SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD	

APPLICANT HEREBY CERTIFIES THE FOLLOWING AND REQUESTS CONSIDERATION UNDER THE AFTER FINAL CONSIDERATION PILOT PROGRAM 2.0 (AFCP 2.0) OF THE ACCOMPANYING RESPONSE UNDER 37 CFR 1.116.

1. The above-identified application is (i) an original utility, plant, or design nonprovisional application filed under 35 U.S.C. 111(a) [a continuing application (*e.g.*, a continuation or divisional application) is filed under 35 U.S.C. 111(a) and is eligible under (i)], or (ii) an international application that has entered the national stage in compliance with 35 U.S.C. 371(c).
2. The above-identified application contains an outstanding final rejection.
3. Submitted herewith is a response under 37 CFR 1.116 to the outstanding final rejection. The response includes an amendment to at least one independent claim, and the amendment does not broaden the scope of the independent claim in any aspect.
4. This certification and request for consideration under AFCP 2.0 is the only AFCP 2.0 certification and request filed in response to the outstanding final rejection.
5. Applicant is willing and available to participate in any interview requested by the examiner concerning the present response.
6. This certification and request is being filed electronically using the Office's electronic filing system (EFS-Web).
7. Any fees that would be necessary consistent with current practice concerning responses after final rejection under 37 CFR 1.116, *e.g.*, extension of time fees, are being concurrently filed herewith. [There is no additional fee required to request consideration under AFCP 2.0.]
8. By filing this certification and request, applicant acknowledges the following:

- Reissue applications and reexamination proceedings are not eligible to participate in AFCP 2.0.
- The examiner will verify that the AFCP 2.0 submission is compliant, *i.e.*, that the requirements of the program have been met (see items 1 to 7 above). For compliant submissions:
    - The examiner will review the response under 37 CFR 1.116 to determine if additional search and/or consideration (i) is necessitated by the amendment and (ii) could be completed within the time allotted under AFCP 2.0. If additional search and/or consideration is required but cannot be completed within the allotted time, the examiner will process the submission consistent with current practice concerning responses after final rejection under 37 CFR 1.116, *e.g.*, by mailing an advisory action.
    - If the examiner determines that the amendment does not necessitate additional search and/or consideration, or if the examiner determines that additional search and/or consideration is required and could be completed within the allotted time, then the examiner will consider whether the amendment places the application in condition for allowance (after completing the additional search and/or consideration, if required). If the examiner determines that the amendment does not place the application in condition for allowance, then the examiner will contact the applicant and request an interview.
        - The interview will be conducted by the examiner, and if the examiner does not have negotiation authority, a primary examiner and/or supervisory patent examiner will also participate.
        - If the applicant declines the interview, or if the interview cannot be scheduled within ten (10) calendar days from the date that the examiner first contacts the applicant, then the examiner will proceed consistent with current practice concerning responses after final rejection under 37 CFR 1.116.

Signature /David N Fogg/	Date January 30, 2014
Name (Print/Typed) David N. Fogg	Practitioner Registration No. 35138

Note: *This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.*

☐ * Total of ________forms are submitted.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	18064891
Application Number:	13415384
International Application Number:	
Confirmation Number:	5259
Title of Invention:	SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD
First Named Inventor/Applicant Name:	Francois Hebert
Customer Number:	94108
Filer:	David Fogg/Jennifer Swanson
Filer Authorized By:	David Fogg
Attorney Docket Number:	125.288US02
Receipt Date:	30-JAN-2014
Filing Date:	08-MAR-2012
Time Stamp:	09:17:57
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		00409812.PDF	133277 8c84ab2a943b73244f10c52af6a54e4ad86f8851	yes	14

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Response After Final Action	1	1
	Claims	2	9
	Applicant Arguments/Remarks Made in an Amendment	10	14

Warnings:

Information:

2	After Final Consideration Program Request	00409826.PDF	172390 8bebb4ee9111c8fb118c3a9be74a0778d9a487c3	no	2

Warnings:

Information:

Total Files Size (in bytes):	305667

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/415,384	Filing Date 03/08/2012	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	NUMBER FILED (Column 1)	NUMBER EXTRA (Column 2)	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter “0” in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	01/30/2014	CLAIMS REMAINING AFTER AMENDMENT (Column 1)		HIGHEST NUMBER PREVIOUSLY PAID FOR (Column 2)	PRESENT EXTRA (Column 3)	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	x $80 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	x $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD’L FEE	**0**

AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT (Column 1)		HIGHEST NUMBER PREVIOUSLY PAID FOR (Column 2)	PRESENT EXTRA (Column 3)	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD’L FEE	

* If the entry in column 1 is less than the entry in column 2, write “0” in column 3.
** If the “Highest Number Previously Paid For” IN THIS SPACE is less than 20, enter “20”.
*** If the “Highest Number Previously Paid For” IN THIS SPACE is less than 3, enter “3”.
The “Highest Number Previously Paid For” (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/TINA M. BELL/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/415,384	03/08/2012	Francois Hebert	125.288US02	5259

94108 7590 12/27/2013
Fogg & Powers LLC/Intersil Americas LLC
5810 W. 78th Street
Minneapolis, MN 55439

EXAMINER	
WILSON, SCOTT R	

ART UNIT	PAPER NUMBER
2826	

NOTIFICATION DATE	DELIVERY MODE
12/27/2013	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketing@fogglaw.com

Office Action Summary	**Application No.** 13/415,384	**Applicant(s)** HEBERT, FRANCOIS	
	Examiner SCOTT R. WILSON	**Art Unit** 2826	**AIA (First Inventor to File) Status** No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *9/18/2013*.
  ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.
3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-20* is/are pending in the application.
  5a) Of the above claim(s) _____ is/are withdrawn from consideration.
6)☐ Claim(s) _____ is/are allowed.
7)☒ Claim(s) *1,6,7,11,12 and 15-17* is/are rejected.
8)☒ Claim(s) *2-5,8-10,13,14 and 18-20* is/are objected to.
9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.
11)☒ The drawing(s) filed on *8 March 2012* is/are: a)☒ accepted or b)☐ objected to by the Examiner.
  Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
  Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
Certified copies:
a)☐ All b)☐ Some** c)☐ None of the:
  1.☐ Certified copies of the priority documents have been received.
  2.☐ Certified copies of the priority documents have been received in Application No. _____.
  3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.
3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
4) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 18 September 2013 have been fully considered but they are not persuasive. Applicant states that “nothing in Nakamura teaches or suggests that the driver circuit 11 forms a portion of a gate of both the high-side transistor and the low-side transistor. “, and that “the driver circuit is connected to a gate of each transistor, but the driver circuit is not part of the gate.” The prior rejection relied on Nakamura to teach “a single conductive structure which forms a portion of a gate of the high side transistor and a portion of a gate of the low side transistor.” Nakamura, Figure 3, shows a physical cross section of the formation of the driver circuit (11) and high side FET (12), with a single conductive structure shown represented by horizontal and vertical lines above the interlayer insulation film layer (38). In an actual device, the conductive structure would comprise wiring layers formed above the interlayer insulation film layer. These wiring layers are within the scope of being a single conductive structure, in that they are physically touching and electrically conducting. The single conductive structure would form *a portion of the gate*, where, for example, the single conductive structure touched a particular gate, for example, gate (37).

Applicant further argues that, “Thus, the driver circuit 11 cannot be part of the gate of the low-side switching element since it is not formed on the same substrate as the low-side element. “ As pointed out in the rejection, Nakamura Figure 16, shows the high side element, the low side element and the conductive structure, embodied as driver circuit (11) all on the same substrate, within the dotted line (paragraph [0088]).

Applicant argues that "Thus, Nakamura teaches that it is not advisable to place a vertical trench type MOSFET on the same substrate as the high side switching element." Nakamura, paragraph [0048], reads "Since the low side switching element 13 has a large influence on the conduction loss, the element is desired to have a low on-state resistance. Therefore, as the low side switching element 13, used is a discrete element, for example, a vertical MOSFET such as a trench type MOS field-effect transistor (hereinafter referred to as "trench MOSFET"). *This is because a trench MOSFET has an on-state resistance lower than that of a lateral MOSFET formed of a power IC, if the withstand voltage is about 30V. In such a case, forming the trench MOSFET and the high side switching element on the same semiconductor substrate is not advisable, since it complicates the process.* (emphasis added) The trench MOSFET is a MOSFET having a trench gate structure in which a gate electrode is buried in a trench formed in a semiconductor layer and the semiconductor layer on side walls of the trench is used as a channel. A vertical MOSFET is a MOSFET in which a current passes from the front surface to the rear surface of the semiconductor substrate." In other words, when Nakamura refers to "In such a case", it is referring to a withstand voltage of about 30V. If the withstand voltage is less than 30V, Nakamura teaches the ability of forming the low-side transistor (13) as a VDMOS, and teaches formation of the low-side transistor (13) on the same substrate as the high-side transistor, in the embodiment of Figure 16.

Applicants argues that “Thus, the blanket implant discussed in paragraph [0044] is within a single device. Nothing in Bhalla teaches or suggests performing an unmasked blanket body implant which covers both a high-side device and a low-side device.”. The teaching of Bhalla was relied on to disclose an unmasked blanket body implant *for whatever device is formed in the die*, in one case a high side device, and in another case, a low side device. Nakamura alone teaches forming a high side device and low side device on the same die.

Applicant states that “Nothing in Bhalla, taken alone or in combination with Nakamura, teaches or suggests the ability to perform an unmasked blanket implant which covers both the high-side device and the low-side device as claimed in claim 1. “ Since Bhalla teaches performing an unmasked blanket implant in a high side device and a low side device, and since Nakamura teaches forming a high side device and low side device on a common die, the combination teaches performing an unmasked blanket implant in a high side device and low side device formed on a common die. The motivation would be change the body profile in the body bottom region and enhance the breakdown voltage without noticeably increasing the transistor on-resistance (Bhalla, paragraph [0044]).

Applicant makes substantially similar arguments regarding claims 12-20, therefore substantially similar responses apply.

Claim Rejections - 35 USC § 103

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 6, 7 and 11 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Nakamura et al. (US 2005/0179472 A1)(Nakamura) in view of Bhalla et al. (US 2009/0065861 A1)(Bhalla). As to claim 1, Nakamura, Figure 16, discloses a method for forming a semiconductor device, the method comprising: forming, on a semiconductor die (paragraph [0088]), a high-side transistor (12) comprising a lateral diffusion metal oxide semiconductor (LDMOS) device (shown on the right-hand-side of Figure 3); forming, on the semiconductor die, a low-side transistor comprising a trench-gate vertical diffusion metal oxide semiconductor (VDMOS) device (paragraph [0048]-[0049] and Figure 4), and forming, on the semiconductor die, a single conductive structure, embodied as the driver circuit (11), which forms a portion of a gate of the high-side transistor and a portion of a gate of the low-side transistor. Nakamura does not disclose expressly performing an unmasked blanket body implant in a layer of the high-side transistor and a layer of the low-side transistor to form high-side and low-side body regions. Bhalla, Figure 7, discloses (paragraph [0044]) an unmasked blanket body implant that may be performed in both the high-side transistor and low-side transistor regions of a power MOS device, which may be a DC/DC converter (paragraph [0002]). At the time of invention, it would have been obvious for one of ordinary skill in the art to perform the unmasked blanket body implant of Bhalla in the method of formation of the power MOS device of Nakamura. The motivation would have been to change the body profile in the body bottom region and enhance the breakdown voltage without noticeably increasing the transistor on-resistance (Bhalla, paragraph [0044]). Therefore, it would have been obvious to combine Nakamura with Bhalla to obtain the method of claim 1.

As to claim 6, Nakamura, Figure 2A, discloses (Abstract and paragraph [0040]) that the low side FET may be formed on a semiconductor die, which may be considered a first semiconductor die, and voltage converter controller circuitry (11) may be formed a second semiconductor die different from the first semiconductor die and that the die containing the voltage converter controller circuitry may be electrically coupled (13) with the first semiconductor die.

As to claim 7, Nakamura, Figure 2A, discloses (paragraph [0047]) co-packaging the first semiconductor die and the second semiconductor die into a single semiconductor device (2)("package").

As to claim 11, Nakamura, Figure 3, discloses (paragraph [0045]) forming a conductive contact within a trench to electrically couple a high-side transistor source (n^+ region 35) and a high-side transistor body (neighboring p^+ region).

Claim 12 and 15-17 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Bhalla. As to claim 12, Nakamura, Figure 16, discloses a method for forming a semiconductor device, the method comprising: forming, on a single semiconductor die (paragraph [0088]), a high-side transistor (12) comprising a lateral diffusion metal oxide semiconductor (LDMOS) device (shown on the right-hand-side of Figure 3); forming, on the semiconductor die, a low-side transistor comprising a trench- gate vertical diffusion metal oxide semiconductor (VDMOS) device (paragraph [0048]-[0049] and Figure 4), and forming a single conductive structure, embodied as the driver circuit (11), which forms a portion of a gate of the high-side transistor and a portion of a gate of the low-side transistor. Nakamura does not disclose expressly that forming the high-side transistor comprises: forming a body region; forming a body contact region in the body region; and forming a trench-substrate-contact (TSC) through the body contact region and the body region such that the TSC contacts a top surface of the body contact region and a side of the body contact region. Bhalla, Figure 6B, discloses an embodiment of a method of formation of a DMOS device, an example of which may be a DC-DC converter (paragraph [0026]), comprising forming a body region (N^-), forming a body contact region (Figure 4P, element 470) in the body region, and forming a trench-substrate-contact (TSC)(608) through the body contact region and the body region such that the TSC contacts a top surface of the body contact region and a side of the body contact region. At the time of invention, it would have been obvious to form the TSC of Bhalla in the method of Nakamura. The motivation would have been to form a punch-through prevention layer (Bhalla, paragraph [0042]). Therefore, it would have been obvious to combine Nakamura with Bhalla to obtain the method of claim 12.

As to claim 15, Bhalla, Figure 4U, discloses that forming the TSC comprises forming the TSC such that the TSC electrically shorts a passivation layer (480), which is within the scope of being a gate shield, for the high-side transistor to the substrate, the

TSC contacting the semiconductor substrate and the body contact region on all sides of a portion of the TSC.

As to claim 16, Nakamura, Figure 2A, discloses (Abstract and paragraph [0040]) that the low side FET may be formed on a semiconductor die, which may be considered a first semiconductor die, and voltage converter controller circuitry (11) may be formed a second semiconductor die different from the first semiconductor die and that the die containing the voltage converter controller circuitry may be electrically coupled (13) with the first semiconductor die.

As to claim 17, Nakamura, Figure 2A, discloses (paragraph [0047]) co-packaging the first semiconductor die and the second semiconductor die into a single semiconductor device (2)("package").

Allowable Subject Matter

Claims 2 and 3 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed method which forms from a single conductive structure a shield for the high-side transistor gate, a contact to a floating guard ring, and a contact to the source of the low-side trench-gate VDMOS transistor.

Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed method which includes forming a conductive trench-source- contact structure which electrically shorts a gate shield for the high-side LDMOS transistor gate to the substrate, which contacts the semiconductor substrate, and which contacts a body contact on all sides of a portion of the trench-source-contact structure.

Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed method which forms contacts to the source and body regions of the high-side and low-side transistors, and a high-side gate shield, all from a single conductive structure.

Claims 8-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed method where a single conductive structure forms a conductive trench contact and a gate shield formed between a gate portion of the high-side LDMOS transistor and a structure overlying the gate shield.

Claims 13 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed method which forms from a single conductive structure a shield for the high-side transistor gate, a contact to a floating guard ring, and a contact to the source of the low-side trench-gate VDMOS transistor.

Claims 18-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed method where a single conductive structure forms a conductive trench contact and a gate shield formed between a gate portion of the high-side LDMOS transistor and a structure overlying the gate shield.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SCOTT R. WILSON whose telephone number is (571)272-1925. The examiner can normally be reached on M-F 8:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Julio Maldonado can be reached on 571-272-1864. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

srw

/TAN N TRAN/
Primary Examiner, Art Unit 2826

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	2	"20050179472".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/05 13:16
S2	0	"KR 20050085461 A"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/05 13:19
S3	0	"KR 1020050085461 A"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/05 13:19
S4	1	"KR 2005085461 A"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/05 13:19
S5	2	"7459750".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/05 13:20
S6	367	ldmos and vdmos	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/05 17:04
S7	49	("20030098468" | "20050179472" | "20050245020" | "20050280163" | "20060231904" | "20070158778" | "20070249092" | "20080023785" | "20080023825" | "20080024102" | "20090039394" | "20090057869" | "20090072368" | "20090263947" | "20100133644" | "20100140693" | "20100155837" | "20100155915" | "4924112" | "5119159" | "5242841" | "6710439" | "6812782" | "6700793").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/05 17:05
S8	5	S6 and S7	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/05 17:05
S9	136	ldmos and vdmos and (shield or cover)	US-PGPUB; USPAT; EPO; JPO;	OR	OFF	2011/04/06 13:50

			DERWENT			
S10	58	ldmos and vdmos and ((shield or cover) with gate)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/06 13:50
S11	10	ldmos and vdmos and (((shield or cover) with gate) same ldmos)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/06 13:51
S12	1	ldmos and vdmos and (((shield or cover) with gate) same ldmos) and (guard adj ring)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/06 13:53
S13	340	ldmos same vdmos	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/06 15:14
S14	324	ldmos with vdmos	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/06 15:14
S15	12142	257/299,213,296,288,334,327,E21.002.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/09 15:05
S16	138	ldmos and vdmos and (shield or cover)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/09 15:05
S17	10	S15 and S16	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/09 15:05
S18	1	"12/320577"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/09 15:26
S19	12507	257/299,213,296,288,334,327,E21.002.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/07/30 19:43
S20	140	ldmos and vdmos and (shield or cover)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/07/30 19:43
S21	0	S19 and S20 and @pd>"20110415"	US-PGPUB; USPAT; EPO; JPO;	OR	OFF	2011/07/30 19:43

			DERWENT			
S23	19967	257/299,213,296,288,334,327,E21.002.ccls. 438/238,239,270,271,386,399.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/07/30 19:54
S24	140	ldmos and vdmos and (shield or cover)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/07/30 19:54
S25	0	S23 and S24 and @pd>"20110415"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/07/30 19:54
S26	6	"12/471911"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/07/30 20:00
S27	6	("7271470" "7566931" "7618896").pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/11/05 22:13
S28	12942	257/299,213,296,288,334,327,E21.002.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/12/13 10:51
S29	150	ldmos and vdmos and (shield or cover)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/12/13 10:51
S30	1	S28 and S29 and @pd>"20110730"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/12/13 10:51
S31	20585	257/299,213,296,288,334,327,E21.002.ccls. 438/238,239,270,271,386,399.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/12/13 10:51
S32	150	ldmos and vdmos and (shield or cover)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/12/13 10:51
S33	1	S31 and S32 and @pd>"20110730"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/12/13 10:51
S35	1	"13/415384"	US-PGPUB; USPAT; EPO; JPO;	OR	ON	2013/07/24 14:40

			DERWENT			
S36	7	(body adj implant$5) same high-side same low-side	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/07/24 16:32
S37	3	"4924112".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/07/24 16:45
S38	2	"6710439".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/07/24 16:46
S39	3	"6700793".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/07/24 16:52
S40	2	"20060231904".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/07/24 16:55
S41	2	"20040125573".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/07/24 17:09
S42	2	"20060231904".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/07/24 17:16
S43	100	("20050245020" | "20070158778" | "20050179472" | "20080023825" | "20090039394" | "20090072368" | "20100133644" | "6812782" | "20090130799" | "20090283919" | "7732929" | "20060231904" | "20050280163" | "20100140693" | "5242841" | "7566931" | "20080203550" | "20080268577" | "6933593" | "7800208" | "20080023785" | "20080024102" | "6700793" | "20020093094" | "7042730" | "20090057869" | "20110024884" | "20030098468" | "20040262678" | "20100155837" | "7618896" | "20070034942" | "20080246086" | "6420780" | "20080017907" | "20070195563" | "6130458" | "6710439" | "7459750" | "20100155836" | "20040125573" | "20070249092" | "20090263947" | "20100155915" | "4924112" | "5119159" | "7271470").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/07/24 17:30
S44	47	("20050245020" | "20070158778" | "20050179472" | "20080023825" | "20090039394" | "20090072368" | "20100133644" | "6812782" |	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/24 17:30

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S45	6	(body with blanket with implant) same ((high-side or (high adj side)) same (low-side or (low adj side)))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/25 09:47
S46	19	(body with blanket with implant) and ((high-side or (high adj side)) same (low-side or (low adj side)))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/25 09:55
S47	13	S46 not S45	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/25 09:55
S48	41	"11/056346"	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/25 10:02
S49	18	"11/900616"	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/25 10:04
S50	5	"12/005130"	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/25 10:07
S51	2	"20090065861".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/07/26 10:01
S52	8	(("20050245020" | "20070158778" | "20050179472" | "20080023825" | "20090039394" | "20090072368" | "20100133644" | "6812782" | "20090130799" | "20090283919" | "7732929" | "20060231904" | "20050280163" | "20100140693" | "5242841" | "7566931" | "20080203550" | "20080268577" | "6933593" | "7800208" | "20080023785" | "20080024102" | "6700793" | "20020093094" | "7042730" | "20090057869" | "20110024884" | "20030098468" | "20040262678" | "20100155837" | "7618896" | "20070034942" | "20080246086" |	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/26 10:14

		"6420780" | "20080017907" | "20070195563" | "6130458" | "6710439" | "7459750" | "20100155836" | "20040125573" | "20070249092" | "20090263947" | "20100155915" | "4924112" | "5119159" | "7271470").PN.) and (shield with gate)				
S53	1	(("20050245020" | "20070158778" | "20050179472" | "20080023825" | "20090039394" | "20090072368" | "20100133644" | "6812782" | "20090130799" | "20090283919" | "7732929" | "20060231904" | "20050280163" | "20100140693" | "5242841" | "7566931" | "20080203550" | "20080268577" | "6933593" | "7800208" | "20080023785" | "20080024102" | "6700793" | "20020093094" | "7042730" | "20090057869" | "20110024884" | "20030098468" | "20040262678" | "20100155837" | "7618896" | "20070034942" | "20080246086" | "6420780" | "20080017907" | "20070195563" | "6130458" | "6710439" | "7459750" | "20100155836" | "20040125573" | "20070249092" | "20090263947" | "20100155915" | "4924112" | "5119159" | "7271470").PN.) and (shield with gate) and (guard with ring)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/26 10:16
S54	4664	transistor same (high-side or (high adj side)) same (low-side or (low adj side))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/26 10:30
S55	96	transistor same (high-side or (high adj side)) same (low-side or (low adj side)) and (shield with gate)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/26 11:01
S56	15	transistor same (high-side or (high adj side)) same (low-side or (low adj side)) and ((shield with gate) same (high-side or (high adj side)))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/26 11:01
S57	24514	257/299,213,296,288,334,327,E21.002.ccls. 438/238,239,270,271,386,399.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2013/07/27 07:33
S58	96	transistor same (high-side or (high adj side)) same (low-side or (low adj side)) and (shield with gate)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/27 07:33
S59	20	S58 and S57	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2013/07/27 07:33
S60	1	"13/415384"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/12/16 15:24

S61	1	(body with blanket with implant) same ((high-side or (high adj side)) same (low-side or (low adj side))) and @pd>"20130724"	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/12/18 14:05
S62	3	(body with blanket with implant) and ((high-side or (high adj side)) same (low-side or (low adj side))) and @pd>"20130724"	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/12/18 14:05
S63	27072	257/299,213,296,288,334,327,E21.002.ccls. 438/238,239,270,271,386,399.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2013/12/18 14:06
S64	97	transistor same (high-side or (high adj side)) same (low-side or (low adj side)) and (shield with gate)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/12/18 14:06
S65	0	S64 and S63 and @pd>"20130724"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2013/12/18 14:06
S66	3	S61 S62	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2013/12/18 14:06

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S22	0	(voltage and converter and output and stage and semiconductor and die and high and side and ldmos and low and side and vdmos and transistor).clm.	USPAT; UPAD	OR	OFF	2011/07/30 19:47
S34	0	(voltage and converter and output and stage and semiconductor and die and high and side and ldmos and low and side and vdmos and transistor).clm.	USPAT; UPAD	OR	OFF	2011/12/13 10:52

12/18/2013 2:09:04 PM
H:\ Workspaces Backup\ 13-415384 - DC-DC Converter CON.wsp

Search Notes	**Application/Control No.** 13415384	**Applicant(s)/Patent Under Reexamination** HEBERT, FRANCOIS
	Examiner SCOTT R WILSON	**Art Unit** 2826

CPC- SEARCHED

Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED

Symbol	Date	Examiner

US CLASSIFICATION SEARCHED

Class	Subclass	Date	Examiner

SEARCH NOTES

Search Notes	Date	Examiner
257/299,213,296,288,334,327,E21.002.ccls. 438/238,239,270,271,386,399.ccls. and text. See search history printout	7/24/2013	srw
257/299,213,296,288,334,327,E21.002.ccls. 438/238,239,270,271,386,399.ccls. and text. See updated search history printout	12/18/2013	srw

INTERFERENCE SEARCH

US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

Applicant(s)	Hebert	**AMENDMENT AND RESPONSE UNDER 37 C.F.R. § 1.111**
Serial No.	13/415,384	
Filing Date	3/8/2012	
Confirmation No.	5259	
Examiner Name	WILSON, SCOTT R.	
Group Art Unit	2826	
Attorney Docket No.	125.288US02	
Title: SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD		

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

The Office Action mailed on August 6, 2013 has been reviewed. Please amend the above-identified application as follows.

Remarks begin on page 2 of this paper.

REMARKS

The Office Action mailed on August 6, 2013 has been reviewed. Claims 1-20 are pending in this application.

Rejections Under 35 U.S.C. § 103

Claims 1, 6, 7 and 11 were rejected under pre-AIA 35 USC § 103(a) as being unpatentable over Nakamura et al. (U.S. Publication No. 2005/0179472) in view of Bhalla et al. (U.S. Publication No. 2009/0065861). Applicant respectfully traverses this rejection.

Claim 1 recites:

> A method for forming a semiconductor device, the method comprising:
>
> forming, on a semiconductor die, a high-side transistor comprising a lateral diffusion metal oxide semiconductor (LDMOS) device;
>
> forming, on the semiconductor die, a low-side transistor comprising a trench-gate vertical diffusion metal oxide semiconductor (VDMOS) device;
>
> forming, on the semiconductor die, a single conductive structure which forms a portion of a gate of the high-side transistor and a portion of a gate of the low-side transistor; and
>
> performing an unmasked blanket body implant in a layer of the high-side transistor and a layer of the low-side transistor to form high-side and low-side body regions.

Nothing in the cited references teaches or suggests all the claimed limitations of claim 1. For example, nothing in the cited references, taken alone or in combination, teaches or suggests "forming, on the semiconductor die, a single conductive structure which forms a portion of a gate of the high-side transistor and a portion of a gate of the low-side transistor." In addressing this limitation, the Examiner relied on the driver circuit 11 of Nakamura. However, nothing in Nakamura teaches or suggests that the driver circuit 11 forms ***a portion*** of a gate of both the high-side transistor and the low-side transistor. For example, with respect to the driver circuit, Nakamura states "a driver circuit 11 is ***connected with*** a gate of a high side MOS field-effect transistor (hereinafter referred to as "high side switching element") 12 and a gate of a low side MOS field-effect transistor (hereinafter referred to as "low side switching element") 13." Para. [0038] (emphasis added). In other words, the driver circuit is connected to a gate of each transistor, but the driver circuit is not part of the gate.

Indeed, the driver circuit shown in Figures 2A and 2B is not formed on the same substrate as the low-side transistor 13. For example, paragraph [0040] of Nakamura states "the driver circuit 11 and the high side switching element 12 are formed on the same semiconductor substrate 1, shown by an enclosed dotted line." Figures 2A and 2B clearly show the low-side switching element outside the dotted lines. Thus, the driver circuit 11 cannot be part of the gate of the low-side switching element since it is not formed on the same substrate as the low-side element.

Furthermore, Nakamura teaches away from forming a low-side VDMOS on the same semiconductor die as a high-side LDMOS. In particular, Nakamura states "as the low side switching element 13, used is a discrete element, for example, a vertical MOSFET such as a trench type MOS field-effect transistor … In such a case, forming the trench MOSFET and the high side switching element on the same semiconductor substrate ***<u>is not advisable</u>***, since it complicates the process." Para. [0048]. Thus, Nakamura teaches that it is not advisable to place a vertical trench type MOSFET on the same substrate as the high side switching element. Indeed, in the only embodiment of Nakamura that includes a low-side device and a high-side device on the same substrate, "the low side switching element 13 is formed of a ***lateral*** MOS field-effect transistor" as shown in Figure 16. Para. [0090] (emphasis added).

Thus, nothing in Nakamura teaches or suggests forming a low-side VDMOS on the same semiconductor die as a high-side LDMOS or "a single conductive structure which forms a portion of a gate of the high-side transistor and a portion of a gate of the low-side transistor." Nothing in Bhalla cures the above defects in Nakamura.

In addition, nothing in Bhalla or Nakamura, taken alone or in combination, teaches or suggests "performing an unmasked blanket body implant in a layer of the high-side transistor and a layer of the low-side transistor to form high-side and low-side body regions." As recited in claim 1, the high-side transistor and the low-side transistor are formed on the same semiconductor die. Additionally, the unmasked blanket body implant is performed in both the high-side device and the low-side device. Thus, in order to be an unmasked blanket body implant, the implant is performed in both the high-side transistor and the low-side transistor without a separate mask over one of the transistors. In other words, the high-side body region and the low-side body region are formed by the same unmasked blanket body implant which covers both the high-side transistor and the low-side transistor as opposed to using separate masks and implants for each of the high-side and low-side transistors. For example, as stated in paragraph [0029] of the present application "This implant is self-aligned as no separate mask is needed." Similarly, as stated in paragraph [0030] of the present application, "This can eliminate the need for a separate mask step to form each device."

In addressing this limitation, the Examiner relied on paragraph [0044] and Fig. 7 of Bhalla. However, nothing in the cited passage or elsewhere in Bhalla teaches or suggests performing an unmasked blanket body implant in both a high-side transistor and a low-side transistor. In particular, each of Figures 1A-1F, 4A-4U, and 7 depict a single DMOS device. For example, Bhalla states "FIGS. 1A-1F illustrate several double-diffused metal oxide semiconductor (DMOS) device embodiments;" "FIGS. 4A-4V are device cross-sectional views illustrating in detail an example fabrication process used for fabricating an MOS device;" and "FIGS. 7-10 illustrate optional modifications to the fabrication process." Bhalla paragraphs [0006], [0009], and [0011]. Similarly, Figure 2 of Bhalla depicts a high side FET device 201 and a low side FET device 207. Paragraph [0026] of Bhalla states that "Low side device 207 can be implemented using devices such as 100, 102, or 104 shown in FIGS. 1A-1F." In other words, Figures 1A-1F, 4A-4U, and 7 each depict a single device. Thus, the blanket implant discussed in paragraph [0044] is within a single device. Nothing in Bhalla teaches or suggests performing an unmasked blanket body implant which covers both a high-side device and a low-side device.

Nothing in the combination of Nakamura and Bhalla cures the defect of Bhalla. In particular, a combination of Nakamura and Bhalla would at best suggest a process of masking the high-side device while performing a blanket implant in the low-side device, or vice versa. Nothing in Bhalla, taken alone or in combination with Nakamura, teaches or suggests the ability to perform an unmasked blanket implant which covers both the high-side device and the low-side device as claimed in claim 1.

Claims 6, 7 and 11 depend from claim 1 and, thus, are allowable for at least the reasons stated above. Since Applicant believes these dependent claims are allowable for at least the above reasons, further response to all rejections have not been put forth in this response. Applicant, however, reserves the right to address said rejections if a further response is filed.

Claims 12 and 15-17 were rejected under pre-AIA 35 USC § 103(a) as being unpatentable over Nakamura et al. (U.S. Publication No. 2005/0179472) in view of Bhalla et al. (U.S. Publication No. 2009/0065861). Applicant respectfully traverses this rejection.

Claim 12 recites:

A method of forming a semiconductor device, the method comprising:

forming a high-side transistor comprising a lateral diffusion metal oxide semiconductor (LDMOS) device on a single semiconductor die;

forming a low-side transistor comprising a trench-gate vertical diffusion metal oxide semiconductor (VDMOS) device on the single semiconductor die; and

forming a single conductive structure which forms a portion of a gate of the high-side transistor and a portion of a gate of the low-side transistor;

wherein forming the high-side transistor comprises:

forming a body region;

forming a body contact region in the body region; and

forming a trench-substrate-contact (TSC) through the body contact region and the body region such that the TSC contacts a top surface of the body contact region and a side of the body contact region.

Nothing in Nakamura or Bhalla, taken alone or in combination teaches or suggests all the claimed limitations of claim 12. As discussed above with respect to claim 1, nothing in Nakamura or Bhalla teaches or suggests forming a low-side VDMOs on the same semiconductor die as a high-side LDMOS or forming a single conductive structure which forms part of a gate of both the high-side device and the low-side device. Therefore, for at least the reasons stated above with respect to claim 1, nothing in Nakamura or Bhalla teaches or suggests "forming a low-side transistor comprising a trench-gate vertical diffusion metal oxide semiconductor (VDMOS) device on the single semiconductor die;" or "forming a single conductive structure which forms a portion of a gate of the high-side transistor and a portion of a gate of the low-side transistor." Therefore, claim 12 is not obvious over Nakamura in view of Bhalla.

Claims 15-17 depend from claim 12 and, thus, are allowable for at least the reasons stated above. Since Applicant believes these dependent claims are allowable for at least the above reasons, further response to all rejections have not been put forth in this response. Applicant, however, reserves the right to address said rejections if a further response is filed.

Allowable Subject Matter

Applicant thanks the Examiner for the indication that claims 2-5, 8-10, 13-14, and 18-20 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

CONCLUSION

Applicant respectfully submits that claims **1-20** are in condition for allowance and notification to that effect is earnestly requested. If necessary, please charge any additional fees or credit overpayments to Deposit Account No. 502432.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at the telephone number listed below.

Respectfully submitted,

Date: September 18, 2013

/David N Fogg/
David N. Fogg
Reg. No. 35138

Attorneys for Applicant
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5810 W. 78th Street, Ste. 100
Minneapolis, MN 55439
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F – (952) 465-0771

Electronic Acknowledgement Receipt

EFS ID:	16886418
Application Number:	13415384
International Application Number:	
Confirmation Number:	5259
Title of Invention:	SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD
First Named Inventor/Applicant Name:	Francois Hebert
Customer Number:	94108
Filer:	David Fogg/Jennifer Swanson
Filer Authorized By:	David Fogg
Attorney Docket Number:	125.288US02
Receipt Date:	18-SEP-2013
Filing Date:	08-MAR-2012
Time Stamp:	14:40:00
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		00388259.PDF	133649 46ccf247e51a1d3df365eb83dcb1c5551c328748	yes	7

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Applicant Arguments/Remarks Made in an Amendment	2	7

Warnings:

Information:

Total Files Size (in bytes):	133649

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/415,384	Filing Date 03/08/2012	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	NUMBER FILED (Column 1)	NUMBER EXTRA (Column 2)	RATE ($)	FEE ($)
☒ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	**380**
☒ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	**620**
☒ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	**250**
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	* 0	x $60 =	**0**
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2 minus 3 =	* 0	x $250 =	**0**
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	**1250**

APPLICATION AS AMENDED – PART II

AMENDMENT	**09/18/2013**	CLAIMS REMAINING AFTER AMENDMENT (Column 1)		HIGHEST NUMBER PREVIOUSLY PAID FOR (Column 2)	PRESENT EXTRA (Column 3)	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	x $80 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	x $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	**0**

AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT (Column 1)		HIGHEST NUMBER PREVIOUSLY PAID FOR (Column 2)	PRESENT EXTRA (Column 3)	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/AJAY R. DAVID/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/415,384	03/08/2012	Francois Hebert	125.288US02	5259

94108 7590 08/06/2013
Fogg & Powers LLC/Intersil Americas LLC
5810 W. 78th Street
Minneapolis, MN 55439

EXAMINER	
WILSON, SCOTT R	
ART UNIT	**PAPER NUMBER**
2826	
NOTIFICATION DATE	**DELIVERY MODE**
08/06/2013	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketing@fogglaw.com

Office Action Summary	Application No. 13/415,384	Applicant(s) HEBERT, FRANCOIS	
	Examiner SCOTT R. WILSON	Art Unit 2826	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 May 2013*.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.
3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1-20* is/are pending in the application.
5a) Of the above claim(s) _____ is/are withdrawn from consideration.
6)☐ Claim(s) _____ is/are allowed.
7)☒ Claim(s) *1,6,7,11,12 and 15-17* is/are rejected.
8)☒ Claim(s) *2-5,8-10,13,14 and 18-20* is/are objected to.
9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.
11)☒ The drawing(s) filed on *08 March 2012* is/are: a)☒ accepted or b)☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some * c)☐ None of the:
1.☐ Certified copies of the priority documents have been received.
2.☐ Certified copies of the priority documents have been received in Application No. _____.
3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date *See Continuation Sheet*.
3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .
4) ☐ Other: _____.

Continuation of Attachment(s) 2). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :3/19/12, 6/15/12, 9/27/12 (two), 12/19/12, 3/15/13, 5/10/13 (seven in total).

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 6, 7 and 11 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Nakamura et al. (US 2005/0179472 A1)(Nakamura) in view of Bhalla et al. (US 2009/0065861 A1)(Bhalla). As to claim 1, Nakamura, Figure 16, discloses a method for forming a semiconductor device, the method comprising: forming, on a semiconductor die (paragraph [0088]), a high-side transistor (12) comprising a lateral diffusion metal oxide semiconductor (LDMOS) device (shown on the right-hand-side of Figure 3); forming, on the semiconductor die, a low-side transistor comprising a trench-gate vertical diffusion metal oxide semiconductor (VDMOS) device (paragraph [0048]-[0049] and Figure 4), and forming, on the semiconductor die, a single conductive structure, embodied as the driver circuit (11), which forms a portion of a gate of the high-side transistor and a portion of a gate of the low-side transistor. Nakamura does not disclose expressly performing an unmasked blanket body implant in a layer of the high-side transistor and a layer of the low-side transistor to form high-side and low-side body regions. Bhalla, Figure 7, discloses (paragraph [0044]) an unmasked blanket body implant that may be performed in both the high-side transistor and low-side transistor regions of a power MOS device, which may be a DC/DC converter (paragraph [0002]). At the time of invention, it would have been obvious for one of ordinary skill in the art to perform the unmasked blanket body implant of Bhalla in the method of formation of the power MOS device of Nakamura. The motivation would have been to change the body profile in the body bottom region and enhance the breakdown voltage without noticeably increasing the transistor on-resistance (Bhalla, paragraph [0044]). Therefore, it would have been obvious to combine Nakamura with Bhalla to obtain the method of claim 1.

As to claim 6, Nakamura, Figure 2A, discloses (Abstract and paragraph [0040]) that the low side FET may be formed on a semiconductor die, which may be considered a first semiconductor die, and voltage converter controller circuitry (11) may be formed a second semiconductor die different from the first semiconductor die and that the die containing the voltage converter controller circuitry may be electrically coupled (13) with the first semiconductor die.

As to claim 7, Nakamura, Figure 2A, discloses (paragraph [0047]) co-packaging the first semiconductor die and the second semiconductor die into a single semiconductor device (2)("package").

As to claim 11, Nakamura, Figure 3, discloses (paragraph [0045]) forming a conductive contact within a trench to electrically couple a high-side transistor source (n^+ region 35) and a high-side transistor body (neighboring p^+ region).

Claim 12 and 15-17 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Bhalla. As to claim 12, Nakamura, Figure 16, discloses a method for forming a semiconductor device, the method comprising:

forming, on a single semiconductor die (paragraph [0088]), a high-side transistor (12) comprising a lateral diffusion metal oxide semiconductor (LDMOS) device (shown on the right-hand-side of Figure 3); forming, on the semiconductor die, a low-side transistor comprising a trench- gate vertical diffusion metal oxide semiconductor (VDMOS) device (paragraph [0048]-[0049] and Figure 4), and forming a single conductive structure, embodied as the driver circuit (11), which forms a portion of a gate of the high-side transistor and a portion of a gate of the low-side transistor. Nakamura does not disclose expressly that forming the high-side transistor comprises: forming a body region; forming a body contact region in the body region; and forming a trench-substrate-contact (TSC) through the body contact region and the body region such that the TSC contacts a top surface of the body contact region and a side of the body contact region. Bhalla, Figure 6B, discloses an embodiment of a method of formation of a DMOS device, an example of which may be a DC-DC converter (paragraph [0026]), comprising forming a body region (N^-), forming a body contact region (Figure 4P, element 470) in the body region, and forming a trench-substrate-contact (TSC)(608) through the body contact region and the body region such that the TSC contacts a top surface of the body contact region and a side of the body contact region. At the time of invention, it would have been obvious to form the TSC of Bhalla in the method of Nakamura. The motivation would have been to form a punch-through prevention layer (Bhalla, paragraph [0042]). Therefore, it would have been obvious to combine Nakamura with Bhalla to obtain the method of claim 12.

As to claim 15, Bhalla, Figure 4U, discloses that forming the TSC comprises forming the TSC such that the TSC electrically shorts a passivation layer (480), which is within the scope of being a gate shield, for the high-side transistor to the substrate, the TSC contacting the semiconductor substrate and the body contact region on all sides of a portion of the TSC.

As to claim 16, Nakamura, Figure 2A, discloses (Abstract and paragraph [0040]) that the low side FET may be formed on a semiconductor die, which may be considered a first semiconductor die, and voltage converter controller circuitry (11) may be formed a second semiconductor die different from the first semiconductor die and that the die containing the voltage converter controller circuitry may be electrically coupled (13) with the first semiconductor die.

As to claim 17, Nakamura, Figure 2A, discloses (paragraph [0047]) co-packaging the first semiconductor die and the second semiconductor die into a single semiconductor device (2)("package").

Allowable Subject Matter

Claims 2 and 3 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed method which forms from a single conductive structure a shield for the high-side transistor gate, a contact to a floating guard ring, and a contact to the source of the low-side trench-gate VDMOS transistor.

Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed method which includes forming a conductive trench-source- contact structure which electrically shorts a gate shield for the high-side LDMOS transistor gate to the substrate, which contacts the semiconductor substrate, and which contacts a body contact on all sides of a portion of the trench-source-contact structure.

Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed method which forms contacts to the source and body regions of the high-side and low-side transistors, and a high-side gate shield, all from a single conductive structure.

Claims 8-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed method where a single conductive structure forms a conductive trench contact and a gate shield formed between a gate portion of the high-side LDMOS transistor and a structure overlying the gate shield.

Claims 13 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed method which forms from a single conductive structure a shield for the high-side transistor gate, a contact to a floating guard ring, and a contact to the source of the low-side trench-gate VDMOS transistor.

Claims 18-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed method where a single conductive structure forms a conductive trench contact and a gate shield formed between a gate portion of the high-side LDMOS transistor and a structure overlying the gate shield.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SCOTT R. WILSON whose telephone number is (571)272-1925. The examiner can normally be reached on M-F 8:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Julio Maldonado can be reached on 571-272-1864. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

srw

/TAN N TRAN/
Primary Examiner, Art Unit 2826

Notice of References Cited	Application/Control No. 13/415,384	Applicant(s)/Patent Under Reexamination HEBERT, FRANCOIS
	Examiner SCOTT R. WILSON	Art Unit 2826 — Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2005/0179472	08-2005	Nakamura et al.	327/109
*	B	US-2009/0065861	03-2009	Bhalla et al.	257/331
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
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	O					
	P					
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	R					
	S					
	T					

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	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	13415384
Filing Date	2012-03-08
First Named Inventor	Hebert
Art Unit	
Examiner Name	S. Wilson
Attorney Docket Number	125.288US02

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.R.W

Receipt date: 05/10/2013	Application Number	13415384	13415384 - GAU: 2826
INFORMATION DISCLOSURE STATEMENT BY APPLICANT **(Not for submission under 37 CFR 1.99)**	Filing Date	2012-03-08	
	First Named Inventor	Hebert	
	Art Unit		
	Examiner Name	S. Wilson	
	Attorney Docket Number	125.288US02	

/S.R.W./	1	CHINESE PATENT OFFICE, "Notice on Grant of Patent Right For Invention", "from Foreign Counterpart of U.S. Application No. 12/477,818 ", 3/26/2013, Page(s) 1-4, Published in: CN	☐
/S.R.W./	2	U.S. PATENT AND TRADEMARK OFFICE, "Final Office Action", "Application Serial No. 13/048,165", 3/19/2013, Page (s) 1-17	☐
/S.R.W./	3	U.S. PATENT AND TRADEMARK OFFICE, "Notice of Allowance", "Application Serial No. 13/048,165", 4/19/2013, Page(s) 1-10	☐

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(Not for submission under 37 CFR 1.99)

Application Number	13415384
Filing Date	2012-03-08
First Named Inventor	Hebert
Art Unit	
Examiner Name	S. Wilson
Attorney Docket Number	125.288US02

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/S.R.W./	1	6420780		2002-07-16	Ko	

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/S.R.W./	1	20070034942		2007-02-15	Xu et al.	
/S.R.W./	2	20080246086		2008-10-09	Korec et al.	
/S.R.W./	3	20100155836		2010-06-24	Hebert	

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Receipt date: 06/15/2012	Application Number	13415384 13415384 - GAU: 2826
INFORMATION DISCLOSURE STATEMENT BY APPLICANT **(Not for submission under 37 CFR 1.99)**	Filing Date	2012-03-08
	First Named Inventor	Hebert
	Art Unit	
	Examiner Name	S. Wilson
	Attorney Docket Number	125.288US02

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/S.R.W./	1	EUROPEAN PATENT OFFICE, "EUROPEAN SEARCH REPORT", mailed 6/1/2012, Published in: EP	☐
/S.R.W./	2	KOREAN INTELLECTUAL PROPERTY OFFICE, "Notice of Allowance", 5/15/2012, Page(s) 1-3	☐

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Application Number	13415384
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First Named Inventor	Hebert
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Examiner Name	S. Wilson
Attorney Docket Number	125.288US02

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/S.R.W./	1	20060231904		2006-10-19	Kocon	

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Receipt date: 09/27/2012

INFORMATION DISCLOSURE STATEMENT BY APPLICANT **(Not for submission under 37 CFR 1.99)**	Application Number		13415384 13415384 - GAU: 2826
	Filing Date		2012-03-08
	First Named Inventor	Hebert	
	Art Unit		
	Examiner Name	S. Wilson	
	Attorney Docket Number		125.288US02

/S.R.W./	1	CHINESE PATENT OFFICE, "First Office Action", 8/2/2012, Page(s) 1-12, Published in: CN	☐

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Search Notes	**Application/Control No.** 13415384	**Applicant(s)/Patent Under Reexamination** HEBERT, FRANCOIS
	Examiner SCOTT R WILSON	**Art Unit** 2826

CPC- SEARCHED

Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED

Symbol	Date	Examiner

US CLASSIFICATION SEARCHED

Class	Subclass	Date	Examiner

SEARCH NOTES

Search Notes	Date	Examiner
257/299,213,296,288,334,327,E21.002.ccls. 438/238,239,270,271,386,399.ccls. and text. See search history printout	7/24/2013	srw

INTERFERENCE SEARCH

US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Application Number	13415384
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Examiner Name	S. Wilson
Attorney Docket Number	125.288US02

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Receipt date: 12/19/2012 **INFORMATION DISCLOSURE STATEMENT BY APPLICANT** (Not for submission under 37 CFR 1.99)	Application Number	13415384 13415384 - GAU: 2826
	Filing Date	2012-03-08
	First Named Inventor	Hebert
	Art Unit	
	Examiner Name	S. Wilson
	Attorney Docket Number	125.288US02

/S.R.W./	1	EUROPEAN PATENT OFFICE, "Partial European Search Report", "from Foreign Counterpart of U.S. Application No. 12/470,229", 2/22/2012, Page(s) 1-6, Published in: EP	☐
/S.R.W./	2	EUROPEAN PATENT OFFICE, "EXTENDED EUROPEAN SEARCH REPORT", "from Foreign Counterpart of U.S. Application No. 12/470,229", 6/1/2012, Page(s) 1-12, Published in: EP	☐
/S.R.W./	3	KOREAN INTELLECTUAL PROPERTY OFFICE, "Notice of Allowance", "from Foreign Counterpart of U.S. Application No. 12/470,229", 11/30/2011, Page(s) 1-3	☐
/S.R.W./	4	U.S. PATENT AND TRADEMARK OFFICE, "Final Office Action", "Application Serial No. 12/470,229", 3/3/2011, Page (s) 1-15	☐
/S.R.W./	5	U.S. PATENT AND TRADEMARK OFFICE, "Notice of Allowance", "Application Serial No. 12/470,229", 12/28/2011, Page(s) 1-12	☐
/S.R.W./	6	U.S. PATENT AND TRADEMARK OFFICE, "Office Action", "Application Serial No. 12/470,229", 5/14/2010, Page(s) 1-7	☐
/S.R.W./	7	U.S. PATENT AND TRADEMARK OFFICE, "Office Action", "Application Serial No. 12/470,229", 10/06/2010, Page(s) 1-9	☐
/S.R.W./	8	U.S. PATENT AND TRADEMARK OFFICE, "Office Action", "Application Serial No. 12/470,229", 9/7/2011, Page(s) 1-12	☐
/S.R.W./	9	U.S. PATENT AND TRADEMARK OFFICE, "Restriction Requirement", "Application Serial No. 12/470,229", 4/19/2010, Page(s) 1-6	☐
/S.R.W./	10	CHINESE PATENT OFFICE, "First Office Action", "from Foreign Counterpart of U.S. Application No. 12/471/911", 8/2/2012, Page(s) 1-12, Published in: CN	☐
/S.R.W./	11	EUROPEAN PATENT OFFICE, "EXTENDED EUROPEAN SEARCH REPORT", "from Foreign Counterpart of U.S. Application No. 12/471,911", 6/1/2012, Page(s) 1-14, Published in: EP	☐

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.R.W

Receipt date: 12/19/2012

13415384 - GAU: 2826

INFORMATION DISCLOSURE STATEMENT BY APPLICANT **(Not for submission under 37 CFR 1.99)**	Application Number		13415384
	Filing Date		2012-03-08
	First Named Inventor	Hebert	
	Art Unit		
	Examiner Name	S. Wilson	
	Attorney Docket Number		125.288US02

/S.R.W./	12	EUROPEAN PATENT OFFICE, "PARTIAL EUROPEAN SEARCH REPORT", "from Foreign Counterpart of U.S. Application No. 12/471,911", 2/21/2012, Page(s) 1-7, Published in: EP	☐
/S.R.W./	13	KOREAN INTELLECTUAL PROPERTY OFFICE, "Notice of Allowance", "from Foreign Counterpart of U.S. Application No. 12/471,911", 5/15/2012, Page(s) 1-3	☐
/S.R.W./	14	KOREAN PATENT OFFICE, "Office Action", "from Foreign Counterpart of U.S. Application Serial No. 12/471,911", 1/2/2012, Page(s) 1-7, Published in: KR	☐
/S.R.W./	15	KOREAN PATENT OFFICE, "Office Action", "from Foreign Counterpart of U.S. Application Serial No. 12/471,911", 3/14/2012, Page(s) 1-8, Published in: KR	☐
/S.R.W./	16	KOREAN PATENT OFFICE, "Office Action", "from Foreign Counterpart of U.S. Application Serial No. 12/471,911", 4/18/2012, Page(s) 1-7, Published in: KR	☐
/S.R.W./	17	U.S. PATENT AND TRADEMARK OFFICE, "Notice of Allowance", "Application Serial No. 12/471,911", 8/5/2011, Page(s) 1-7	☐
/S.R.W./	18	U.S. PATENT AND TRADEMARK OFFICE, "Notice of Allowance", "Application Serial No. 12/471,911", 1/3/2012, Page(s) 1-12	☐
/S.R.W./	19	U.S. PATENT AND TRADEMARK OFFICE, "Office Action", "Application Serial No. 12/471,911", 4/15/2011, Page(s) 1-19	☐
/S.R.W./	20	CHINESE PATENT OFFICE, "Office Action", "from Foreign Counterpart of U.S. Application No. 12/477,818", 12/7/2011, Published in: CN	☐
/S.R.W./	21	CHINESE PATENT OFFICE, "Office Action", "from Foreign Counterpart of U.S. Application No. 12/477,818", 10/17/2012, Page(s) 1-16, Published in: CN	☐
/S.R.W./	22	U.S. PATENT AND TRADEMARK OFFICE, "Notice of Allowance", "Application Serial No. 12/477,818", 10/29/2010, Page(s) 1-13	☐

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.R.W

Receipt date: 12/19/2012

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	13415384 13415384 - GAU: 2826
Filing Date	2012-03-08
First Named Inventor	Hebert
Art Unit	
Examiner Name	S. Wilson
Attorney Docket Number	125.288US02

/S.R.W./	23	U.S. PATENT AND TRADEMARK OFFICE, "Notice of Allowance", "Application Serial No.12/477,818", 2/22/2011, Page(s) 1-13	☐
/S.R.W./	24	U.S. PATENT AND TRADEMARK OFFICE, "Restriction Requirement", "Application Serial No. 12/477,818 ", 7/6/2010, Page(s) 1-7	☐

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Examiner Signature	/Scott Wilson/	Date Considered	07/27/2013

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(**Not for submission under 37 CFR 1.99**)

Application Number	13415384
Filing Date	2012-03-08
First Named Inventor	Hebert
Art Unit	
Examiner Name	S. Wilson
Attorney Docket Number	125.288US02

U.S.PATENTS

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Receipt date: 03/15/2013

13415384 - GAU: 2826

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	13415384
Filing Date	2012-03-08
First Named Inventor	Hebert
Art Unit	
Examiner Name	S. Wilson
Attorney Docket Number	125.288US02

/S.R.W./	1	EUROPEAN PATENT OFFICE, "Office Action", "from Foreign Counterpart of U.S. Application No. 12/470,229", 2/12/2013, Page(s) 1-5, Published in: EP	☐
/S.R.W./	2	CHINESE PATENT OFFICE, "Office Action", "from Foreign Counterpart of U.S. Application No. 12/471,911 ", 1/28/2013, Page(s) 1-7, Published in: CN	☐
/S.R.W./	3	EUROPEAN PATENT OFFICE, "Office Action", "from Foreign Counterpart of U.S. Application No. 12/471,911", 2/12/2013, Page(s) 1-5, Published in: EP	☐
/S.R.W./	4	KOREAN INTELLECTUAL PROPERTY OFFICE, "Notice of Allowance", "from Foreign Counterpart of U.S. Application Serial No. 12/471,911", 1/29/2013, Page(s) 1-3	☐

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.R.W

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	2	"20050179472".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/05 13:16
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S3	0	"KR 1020050085461 A"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/05 13:19
S4	1	"KR 2005085461 A"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/05 13:19
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S9	136	ldmos and vdmos and (shield or cover)	US-PGPUB; USPAT; EPO; JPO;	OR	OFF	2011/04/06 13:50

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S10	58	ldmos and vdmos and ((shield or cover) with gate)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/06 13:50
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S12	1	ldmos and vdmos and (((shield or cover) with gate) same ldmos) and (guard adj ring)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/06 13:53
S13	340	ldmos same vdmos	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/06 15:14
S14	324	ldmos with vdmos	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/04/06 15:14
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S38	2	"6710439".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/07/24 16:46
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S46	19	(body with blanket with implant) and ((high-side or (high adj side)) same (low-side or (low adj side)))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/25 09:55
S47	13	S46 not S45	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/25 09:55
S48	41	"11/056346"	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/25 10:02
S49	18	"11/900616"	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/25 10:04
S50	5	"12/005130"	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/25 10:07
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S53	1	(("20050245020" | "20070158778" | "20050179472" | "20080023825" | "20090039394" | "20090072368" | "20100133644" | "6812782" | "20090130799" | "20090283919" | "7732929" | "20060231904" | "20050280163" | "20100140693" | "5242841" | "7566931" | "20080203550" | "20080268577" | "6933593" | "7800208" | "20080023785" | "20080024102" | "6700793" | "20020093094" | "7042730" | "20090057869" | "20110024884" | "20030098468" | "20040262678" | "20100155837" | "7618896" | "20070034942" | "20080246086" | "6420780" | "20080017907" | "20070195563" | "6130458" | "6710439" | "7459750" | "20100155836" | "20040125573" | "20070249092" | "20090263947" | "20100155915" | "4924112" | "5119159" | "7271470").PN.) and (shield with gate) and (guard with ring)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/26 10:16
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S55	96	transistor same (high-side or (high adj side)) same (low-side or (low adj side)) and (shield with gate)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/26 11:01
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S57	24514	257/299,213,296,288,334,327,E21.002.ccls. 438/238,239,270,271,386,399.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2013/07/27 07:33
S58	96	transistor same (high-side or (high adj side)) same (low-side or (low adj side)) and (shield with gate)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2013/07/27 07:33
S59	20	S58 and S57	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2013/07/27 07:33

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp

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7/ 27/ 2013 7:36:31 AM
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	13415384
Filing Date	2012-03-08
First Named Inventor	Hebert
Art Unit	
Examiner Name	S. Wilson
Attorney Docket Number	125.288US02

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code1	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/S.R.W./	1	4924112		1990-05-08	Anderson et al.	
/S.R.W./	2	5119159		1992-06-02	Hoshi	
/S.R.W./	3	5242841		1993-09-07	Smayling et al.	
/S.R.W./	4	6130458		2000-10-10	Takagi et al.	
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/S.R.W./	6	6710439		2004-03-23	Lee et al.	
/S.R.W./	7	6812782		2004-11-02	Grant	
/S.R.W./	8	7271470		2007-09-18	Otremba	

Receipt date: 03/19/2012	Application Number	13415384 13415384 - GAU: 2826
INFORMATION DISCLOSURE STATEMENT BY APPLICANT **(Not for submission under 37 CFR 1.99)**	Filing Date	2012-03-08
	First Named Inventor	Hebert
	Art Unit	
	Examiner Name	S. Wilson
	Attorney Docket Number	125.288US02

/S.R.W./	9	7459750		2008-12-02	Ludikhuize	
/S.R.W./	10	7566931		2009-07-28	Kocon	
/S.R.W./	11	7618896		2009-11-17	Joshi et al.	

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/S.R.W./	1	20030098468		2003-05-29	Wheeler et al.	
/S.R.W./	2	20040262678		2004-12-30	Nakazawa et al.	
/S.R.W./	3	20050179472		2005-08-18	Nakamura et al.	
/S.R.W./	4	20050245020		2005-11-03	Zhu et al.	
/S.R.W./	5	20050280163		2005-12-22	Schaffer et al.	
/S.R.W./	6	20070158778		2007-07-12	Kitabatake et al.	

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Application Number	13415384
Filing Date	2012-03-08
First Named Inventor	Hebert
Art Unit	
Examiner Name	S. Wilson
Attorney Docket Number	125.288US02

/S.R.W./	7	20070195563		2007-08-23	Shiraishi et al.	
/S.R.W./	8	20070249092		2007-10-25	Joshi et al.	
/S.R.W./	9	20080023785		2008-01-31	Hebert	
/S.R.W./	10	20080023825		2008-01-31	Hebert et al.	
/S.R.W./	11	20080024102		2008-01-31	Hebert et al.	
/S.R.W./	12	20090039394		2009-02-12	UNO et al.	
/S.R.W./	13	20090057869		2009-03-05	Hebert et al.	
/S.R.W./	14	20090072368		2009-03-19	Hu et al.	
/S.R.W./	15	20090263947		2009-10-22	Hebert	
/S.R.W./	16	20100133644		2010-06-03	Hebert	
/S.R.W./	17	20100140693		2010-06-10	Hebert	

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	Filing Date	2012-03-08	
	First Named Inventor	Hebert	
	Art Unit		
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	Attorney Docket Number	125.288US02	

/S.R.W./	18	20100155837		2010-06-24	Hebert	
/S.R.W./	19	20100155915		2010-06-24	Bell et al.	

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/S.R.W./	1	6933593		2005-08-23	Fissore et al.	
/S.R.W./	2	7042730		2006-05-09	Vaysse et al.	
/S.R.W./	3	7732929		2010-06-08	Otremba et al.	
/S.R.W./	4	7800208		2010-09-21	Otremba	

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/S.R.W./	1	20020093094		2002-07-18	Takagawa et al.	
/S.R.W./	2	20040125573		2004-07-01	Joshi et al.	

Receipt date: 09/27/2012	Application Number	13415384 13415384 - GAU: 2826
INFORMATION DISCLOSURE STATEMENT BY APPLICANT **(Not for submission under 37 CFR 1.99)**	Filing Date	2012-03-08
	First Named Inventor	Hebert
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	Examiner Name	S. Wilson
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/S.R.W./	3	20080017907		2008-01-24	Otremba	
/S.R.W./	4	20080203550		2008-08-28	Ewe et al.	
/S.R.W./	5	20080268577		2008-10-30	Kagii et al.	
/S.R.W./	6	20090057869		2009-03-05	Hebert et al.	
/S.R.W./	7	20090130799		2009-05-21	Havanur	
/S.R.W./	8	20090283919		2009-11-19	Tsui et al.	
/S.R.W./	9	20110024884		2011-02-03	Xue et al.	

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	Attorney Docket Number	125.288US02

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/S.R.W./	1	CHINESE PATENT OFFICE, "First Office Action", "from Foreign Counterpart of U.S. Application No. 12/470,229", 8/3/2012, Page(s) 1-15, Published in: CN	☐
/S.R.W./	2	U.S. PATENT AND TRADEMARK OFFICE, "Office Action", "Application Serial No. 13/048,165", 9/7/2012, Page(s) 1-33	☐

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Doc code: IDS
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	Filing Date	2012-03-08	
	First Named Inventor	Hebert	
	Art Unit		
	Examiner Name		
	Attorney Docket Number	125.288US02	

	1	CHINESE PATENT OFFICE, "Notice on Grant of Patent Right For Invention", "from Foreign Counterpart of U.S. Application No. 12/477,818 ", 3/26/2013, Page(s) 1-4, Published in: CN	☐
	2	U.S. PATENT AND TRADEMARK OFFICE, "Final Office Action", "Application Serial No. 13/048,165", 3/19/2013, Page (s) 1-17	☐
	3	U.S. PATENT AND TRADEMARK OFFICE, "Notice of Allowance", "Application Serial No. 13/048,165", 4/19/2013, Page(s) 1-10	☐

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	Attorney Docket Number	125.288US02

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EFS ID:	15745113
Application Number:	13415384
International Application Number:	
Confirmation Number:	5259
Title of Invention:	SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD
First Named Inventor/Applicant Name:	Francois Hebert
Customer Number:	94108
Filer:	Jay Alan Wahlquist/Robert Thrumston
Filer Authorized By:	Jay Alan Wahlquist
Attorney Docket Number:	125.288US02
Receipt Date:	10-MAY-2013
Filing Date:	08-MAR-2012
Time Stamp:	15:39:07
Application Type:	Utility under 35 USC 111(a)

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	Attorney Docket Number		125.288US02

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	4	KOREAN INTELLECTUAL PROPERTY OFFICE, "Notice of Allowance", "from Foreign Counterpart of U.S. Application Serial No. 12/471,911", 1/29/2013, Page(s) 1-3	☐

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Signature	/Jay Wahlquist/	Date (YYYY-MM-DD)	2013-03-08
Name/Print	Wahlquist, Jay A.	Registration Number	55705

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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EFS ID:	15200007
Application Number:	13415384
International Application Number:	
Confirmation Number:	5259
Title of Invention:	SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD
First Named Inventor/Applicant Name:	Francois Hebert
Customer Number:	94108
Filer:	Jay Alan Wahlquist/Robert Thrumston
Filer Authorized By:	Jay Alan Wahlquist
Attorney Docket Number:	125.288US02
Receipt Date:	15-MAR-2013
Filing Date:	08-MAR-2012
Time Stamp:	09:38:34
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	00353085.PDF	771012 c22afee8129659589246d69d21f1ab256f1adb8f	no	4

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3	Non Patent Literature	00353160.PDF	3616860 fb8efe1bef0305a5eb9e485b50e16571a784d75e	no	7
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4	Non Patent Literature	00350744.PDF	433263 091eb307817ac2ede4a309c8ab44d8cb726aa3d3	no	5
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(**Not for submission under 37 CFR 1.99)**

Application Number	13415384
Filing Date	2012-03-08
First Named Inventor	Hebert
Art Unit	
Examiner Name	
Attorney Docket Number	125.288US02

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	Application Number	13415384
	Filing Date	2012-03-08
	First Named Inventor	Hebert
	Art Unit	
	Examiner Name	
	Attorney Docket Number	125.288US02

	1	EUROPEAN PATENT OFFICE, "Partial European Search Report", "from Foreign Counterpart of U.S. Application No. 12/470,229", 2/22/2012, Page(s) 1-6, Published in: EP	☐
	2	EUROPEAN PATENT OFFICE, "EXTENDED EUROPEAN SEARCH REPORT", "from Foreign Counterpart of U.S. Application No. 12/470,229", 6/1/2012, Page(s) 1-12, Published in: EP	☐
	3	KOREAN INTELLECTUAL PROPERTY OFFICE, "Notice of Allowance", "from Foreign Counterpart of U.S. Application No. 12/470,229", 11/30/2011, Page(s) 1-3	☐
	4	U.S. PATENT AND TRADEMARK OFFICE, "Final Office Action", "Application Serial No. 12/470,229", 3/3/2011, Page (s) 1-15	☐
	5	U.S. PATENT AND TRADEMARK OFFICE, "Notice of Allowance", "Application Serial No. 12/470,229", 12/28/2011, Page(s) 1-12	☐
	6	U.S. PATENT AND TRADEMARK OFFICE, "Office Action", "Application Serial No. 12/470,229", 5/14/2010, Page(s) 1-7	☐
	7	U.S. PATENT AND TRADEMARK OFFICE, "Office Action", "Application Serial No. 12/470,229", 10/06/2010, Page(s) 1-9	☐
	8	U.S. PATENT AND TRADEMARK OFFICE, "Office Action", "Application Serial No. 12/470,229", 9/7/2011, Page(s) 1-12	☐
	9	U.S. PATENT AND TRADEMARK OFFICE, "Restriction Requirement", "Application Serial No. 12/470,229", 4/19/2010, Page(s) 1-6	☐
	10	CHINESE PATENT OFFICE, "First Office Action", "from Foreign Counterpart of U.S. Application No. 12/471/911", 8/2/2012, Page(s) 1-12, Published in: CN	☐
	11	EUROPEAN PATENT OFFICE, "EXTENDED EUROPEAN SEARCH REPORT", "from Foreign Counterpart of U.S. Application No. 12/471,911", 6/1/2012, Page(s) 1-14, Published in: EP	☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT **(Not for submission under 37 CFR 1.99)**	Application Number	13415384
	Filing Date	2012-03-08
	First Named Inventor	Hebert
	Art Unit	
	Examiner Name	
	Attorney Docket Number	125.288US02

	12	EUROPEAN PATENT OFFICE, "PARTIAL EUROPEAN SEARCH REPORT", "from Foreign Counterpart of U.S. Application No. 12/471,911", 2/21/2012, Page(s) 1-7, Published in: EP	☐
	13	KOREAN INTELLECTUAL PROPERTY OFFICE, "Notice of Allowance", "from Foreign Counterpart of U.S. Application No. 12/471,911", 5/15/2012, Page(s) 1-3	☐
	14	KOREAN PATENT OFFICE, "Office Action", "from Foreign Counterpart of U.S. Application Serial No. 12/471,911", 1/2/2012, Page(s) 1-7, Published in: KR	☐
	15	KOREAN PATENT OFFICE, "Office Action", "from Foreign Counterpart of U.S. Application Serial No. 12/471,911", 3/14/2012, Page(s) 1-8, Published in: KR	☐
	16	KOREAN PATENT OFFICE, "Office Action", "from Foreign Counterpart of U.S. Application Serial No. 12/471,911", 4/18/2012, Page(s) 1-7, Published in: KR	☐
	17	U.S. PATENT AND TRADEMARK OFFICE, "Notice of Allowance", "Application Serial No. 12/471,911", 8/5/2011, Page (s) 1-7	☐
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	19	U.S. PATENT AND TRADEMARK OFFICE, "Office Action", "Application Serial No. 12/471,911", 4/15/2011, Page(s) 1-19	☐
	20	CHINESE PATENT OFFICE, "Office Action", "from Foreign Counterpart of U.S. Application No. 12/477,818", 12/7/2011, Published in: CN	☐
	21	CHINESE PATENT OFFICE, "Office Action", "from Foreign Counterpart of U.S. Application No. 12/477,818", 10/17/2012, Page(s) 1-16, Published in: CN	☐
	22	U.S. PATENT AND TRADEMARK OFFICE, "Notice of Allowance", "Application Serial No. 12/477,818", 10/29/2010, Page(s) 1-13	☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13415384
	Filing Date	2012-03-08
	First Named Inventor	Hebert
	Art Unit	
	Examiner Name	
	Attorney Docket Number	125.288US02

	23	U.S. PATENT AND TRADEMARK OFFICE, "Notice of Allowance", "Application Serial No.12/477,818", 2/22/2011, Page(s) 1-13	☐
	24	U.S. PATENT AND TRADEMARK OFFICE, "Restriction Requirement", "Application Serial No. 12/477,818 ", 7/6/2010, Page(s) 1-7	☐

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Application Number	13415384
	Filing Date	2012-03-08
	First Named Inventor	Hebert
	Art Unit	
	Examiner Name	
	Attorney Docket Number	125.288US02

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Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

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A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Jay Wahlquist/	Date (YYYY-MM-DD)	2012-12-19
Name/Print	Wahlquist, Jay A.	Registration Number	55705

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Electronic Acknowledgement Receipt

EFS ID:	14502638
Application Number:	13415384
International Application Number:	
Confirmation Number:	5259
Title of Invention:	SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD
First Named Inventor/Applicant Name:	Francois Hebert
Customer Number:	94108
Filer:	Jay Alan Wahlquist/Robert Thrumston
Filer Authorized By:	Jay Alan Wahlquist
Attorney Docket Number:	125.288US02
Receipt Date:	19-DEC-2012
Filing Date:	08-MAR-2012
Time Stamp:	14:28:24
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
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9	Non Patent Literature	00330820.PDF	207718 1dbf8f81d4337f3926e0c0a88511fbce5d3991b3	no	6
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24	Non Patent Literature	00330813.PDF	241135 cd9270ae7d5546799462d02b546333c007fcc20d	no	7
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25	Information Disclosure Statement (IDS) Form (SB08)	00332120.PDF	906089 836658f7653d2603381ec2597f19365d0b739dd2	no	6
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Filing Date	2012-03-08
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Attorney Docket Number	125.288US02

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	1	6933593		2005-08-23	Fissore et al.	
	2	7042730		2006-05-09	Vaysse et al.	
	3	7732929		2010-06-08	Otremba et al.	
	4	7800208		2010-09-21	Otremba	

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Examiner Initial*	Cite No	Publication Number	Kind Code1	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20020093094		2002-07-18	Takagawa et al.	
	2	20040125573		2004-07-01	Joshi et al.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	13415384
	Filing Date	2012-03-08
	First Named Inventor	Hebert
	Art Unit	
	Examiner Name	
	Attorney Docket Number	125.288US02

	3	20080017907		2008-01-24	Otremba	
	4	20080203550		2008-08-28	Ewe et al.	
	5	20080268577		2008-10-30	Kagii et al.	
	6	20090057869		2009-03-05	Hebert et al.	
	7	20090130799		2009-05-21	Havanur	
	8	20090283919		2009-11-19	Tsui et al.	
	9	20110024884		2011-02-03	Xue et al.	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT **(Not for submission under 37 CFR 1.99)**	Application Number	13415384	
	Filing Date	2012-03-08	
	First Named Inventor	Hebert	
	Art Unit		
	Examiner Name		
	Attorney Docket Number	125.288US02	

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T5
	1	CHINESE PATENT OFFICE, "First Office Action", "from Foreign Counterpart of U.S. Application No. 12/470,229", 8/3/2012, Page(s) 1-15, Published in: CN	☐
	2	U.S. PATENT AND TRADEMARK OFFICE, "Office Action", "Application Serial No. 13/048,165", 9/7/2012, Page(s) 1-33	☐

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# INFORMATION DISCLOSURE STATEMENT BY APPLICANT **(Not for submission under 37 CFR 1.99)**		
	Application Number	13415384
	Filing Date	2012-03-08
	First Named Inventor	Hebert
	Art Unit	
	Examiner Name	
	Attorney Docket Number	125.288US02

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

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OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Jay Wahlquist/	Date (YYYY-MM-DD)	2012-09-27
Name/Print	Wahlquist, Jay A.	Registration Number	55705

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	13849186
Application Number:	13415384
International Application Number:	
Confirmation Number:	5259
Title of Invention:	SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD
First Named Inventor/Applicant Name:	Francois Hebert
Customer Number:	94108
Filer:	Jay Alan Wahlquist/Robert Thrumston
Filer Authorized By:	Jay Alan Wahlquist
Attorney Docket Number:	125.288US02
Receipt Date:	27-SEP-2012
Filing Date:	08-MAR-2012
Time Stamp:	16:23:47
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	00322210.PDF	855883 4831932da307206003c7c768b95f62f918f4c8a0	no	5

Warnings:

Information:

2	Non Patent Literature	00319506.PDF	1416628 90a3c133949ce959a48bac2b127c80f022b97001	no	33
Warnings:					
Information:					
3	Non Patent Literature	00322746.PDF	752890 9412224c77535609d69861e43672a78d98013b6b	no	15
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(**Not for submission under 37 CFR 1.99)**

Application Number	13415384
Filing Date	2012-03-08
First Named Inventor	Hebert
Art Unit	
Examiner Name	
Attorney Docket Number	125.288US02

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Examiner Initial*	Cite No	Patent Number	Kind Code1	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Publication Number	Kind Code1	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20060231904		2006-10-19	Kocon	

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Examiner Initial*	Cite No	Foreign Document Number3	Country Code2 i	Kind Code4	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T5
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	Filing Date	2012-03-08
	First Named Inventor	Hebert
	Art Unit	
	Examiner Name	
	Attorney Docket Number	125.288US02

	1	CHINESE PATENT OFFICE, "First Office Action", 8/2/2012, Page(s) 1-12, Published in: CN	☐

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	Filing Date		2012-03-08
	First Named Inventor	Hebert	
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	Examiner Name		
	Attorney Docket Number		125.288US02

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Signature	/Jay Wahlquist/	Date (YYYY-MM-DD)	2012-09-27
Name/Print	Wahlquist, Jay A.	Registration Number	55705

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Electronic Acknowledgement Receipt

EFS ID:	13857319
Application Number:	13415384
International Application Number:	
Confirmation Number:	5259
Title of Invention:	SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD
First Named Inventor/Applicant Name:	Francois Hebert
Customer Number:	94108
Filer:	Jay Alan Wahlquist/Robert Thrumston
Filer Authorized By:	Jay Alan Wahlquist
Attorney Docket Number:	125.288US02
Receipt Date:	27-SEP-2012
Filing Date:	08-MAR-2012
Time Stamp:	17:02:18
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	00322168.PDF	754940 9ff95c62aa382992467c7c428556cabf1c049d23	no	4

Warnings:

Information:

2	Non Patent Literature	00322750.PDF	6342125 a81e460d17cafcda993d3856a17432ced3b0219a	no	12
Warnings:					
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			Total Files Size (in bytes):	7097065	

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/415,384	03/08/2012	Francois Hebert	125.288US02

CONFIRMATION NO. 5259

PUBLICATION NOTICE

OC000000055203275

94108
Fogg & Powers LLC/Intersil Americas LLC
5810 W. 78th Street
Minneapolis, MN 55439

Title:SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD

Publication No.US-2012-0171817-A1
Publication Date:07/05/2012

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In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

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Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	13415384
Filing Date	2012-03-08
First Named Inventor	Hebert
Art Unit	
Examiner Name	
Attorney Docket Number	125.288US02

U.S.PATENTS

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Examiner Initial*	Cite No	Patent Number	Kind Code1	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6420780		2002-07-16	Ko	

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Examiner Initial*	Cite No	Publication Number	Kind Code1	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20070034942		2007-02-15	Xu et al.	
	2	20080246086		2008-10-09	Korec et al.	
	3	20100155836		2010-06-24	Hebert	

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Examiner Initial*	Cite No	Foreign Document Number3	Country Code2 i	Kind Code4	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T5
	1							☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT **(Not for submission under 37 CFR 1.99)**	Application Number		13415384
	Filing Date		2012-03-08
	First Named Inventor	Hebert	
	Art Unit		
	Examiner Name		
	Attorney Docket Number		125.288US02

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T5
	1	EUROPEAN PATENT OFFICE, "EUROPEAN SEARCH REPORT", mailed 6/1/2012, Published in: EP	☐
	2	KOREAN INTELLECTUAL PROPERTY OFFICE, "Notice of Allowance", 5/15/2012, Page(s) 1-3	☐

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Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13415384
	Filing Date	2012-03-08
	First Named Inventor	Hebert
	Art Unit	
	Examiner Name	
	Attorney Docket Number	125.288US02

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☒ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Jay Wahlquist/	Date (YYYY-MM-DD)	2012-06-15
Name/Print	Wahlquist, Jay A.	Registration Number	55705

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Applicant(s)	Hebert	CERTIFICATION STATEMENT
Serial No.	13/415,384	
Filing Date	3/8/2012	
Group Art Unit		
Examiner Name		
Confirmation No.	5259	
Attorney Docket No.	125.288US02	
Title: SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD		

Applicant respectfully states that:

[x] That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart application and that this communication was not received by any individual designated in § 1.56(c) more than thirty days prior to the filing of the information disclosure statement.

[x] That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at 952-465-0770.

Respectfully submitted,

/Jay Wahlquist/

Date: June 15, 2012

Jay A. Wahlquist
Reg. No. 55705

Attorneys for Applicant
Fogg & Powers LLC
5810 W. 78th St. Ste 100
Minneapolis, MN 55439
T – (952) 465-0770 | F – (952) 465-0771

Electronic Acknowledgement Receipt

EFS ID:	13030080
Application Number:	13415384
International Application Number:	
Confirmation Number:	5259
Title of Invention:	SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD
First Named Inventor/Applicant Name:	Francois Hebert
Customer Number:	94108
Filer:	Jay Alan Wahlquist/Robert Thrumston
Filer Authorized By:	Jay Alan Wahlquist
Attorney Docket Number:	125.288US02
Receipt Date:	15-JUN-2012
Filing Date:	08-MAR-2012
Time Stamp:	17:06:05
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	00307248.PDF	781035 e7fbfece6d42cae403e5be7f5520562f0dc1253c	no	4

Warnings:

Information:

2	Miscellaneous Incoming Letter	00307249.PDF	56392 27fcc3d3eb7171a8396461a48ac80931c14521bc	no	1
Warnings:					
Information:					
3	Non Patent Literature	00307250.PDF	2073384 f501e8c20a086b963f60f6cc97f247cc86899f02	no	14
Warnings:					
Information:					
4	Non Patent Literature	00307088.PDF	196310 70d423ca8e21efcb5b12cefdae200256c9fbfd81	no	3
Warnings:					
Information:					
		Total Files Size (in bytes):	3107121		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number
13/415,384

APPLICATION AS FILED - PART I

	(Column 1)	(Column 2)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE($)	FEE($)		RATE($)	FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	380
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	620
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	250
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*			OR	x 60 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2 minus 3 =	*				x 250 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
			TOTAL			TOTAL	1250

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1)		(Column 2)	(Column 3)					
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
13/415,384	03/08/2012	2811	1250	125.288US02	20	2

CONFIRMATION NO. 5259

FILING RECEIPT

OC000000053357415

94108
Fogg & Powers LLC/Intersil Americas LLC
5810 W. 78th Street
Minneapolis, MN 55439

Date Mailed: 03/28/2012

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Francois Hebert, San Mateo, CA;

Assignment For Published Patent Application

INTERSIL AMERICAS INC., Milpitas, CA

Power of Attorney: The patent practitioners associated with Customer Number 94108

Domestic Priority data as claimed by applicant

This application is a CON of 12/471,911 05/26/2009
which claims benefit of 61/140,610 12/23/2008
and claims benefit of 61/162,232 03/20/2009

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.)

Permission to Access - A proper **Authorization to Permit Access to Application by Participating Offices** (PTO/SB/39 or its equivalent) has been received by the USPTO.

If Required, Foreign Filing License Granted: 03/26/2012

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/415,384**

Projected Publication Date: 07/05/2012

Non-Publication Request: No

Early Publication Request: No

Title

SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD

Preliminary Class

257

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/415,384	03/08/2012	Francois Hebert	125.288US02

CONFIRMATION NO. 5259

POA ACCEPTANCE LETTER

94108
Fogg & Powers LLC/Intersil Americas LLC
5810 W. 78th Street
Minneapolis, MN 55439

OC000000053344923

Date Mailed: 03/28/2012

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 03/08/2012.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/dpham/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(**Not for submission under 37 CFR 1.99)**

Application Number	13415384
Filing Date	2012-03-08
First Named Inventor	Hebert
Art Unit	
Examiner Name	
Attorney Docket Number	125.288US02

U.S.PATENTS

Remove

Examiner Initial*	Cite No	Patent Number	Kind Code1	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	4924112		1990-05-08	Anderson et al.	
	2	5119159		1992-06-02	Hoshi	
	3	5242841		1993-09-07	Smayling et al.	
	4	6130458		2000-10-10	Takagi et al.	
	5	6700793		2004-03-02	Takagawa et al.	
	6	6710439		2004-03-23	Lee et al.	
	7	6812782		2004-11-02	Grant	
	8	7271470		2007-09-18	Otremba	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Application Number		13415384
	Filing Date		2012-03-08
	First Named Inventor	Hebert	
	Art Unit		
	Examiner Name		
	Attorney Docket Number		125.288US02

	9	7459750		2008-12-02	Ludikhuize	
	10	7566931		2009-07-28	Kocon	
	11	7618896		2009-11-17	Joshi et al.	

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Examiner Initial*	Cite No	Publication Number	Kind Code1	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20030098468		2003-05-29	Wheeler et al.	
	2	20040262678		2004-12-30	Nakazawa et al.	
	3	20050179472		2005-08-18	Nakamura et al.	
	4	20050245020		2005-11-03	Zhu et al.	
	5	20050280163		2005-12-22	Schaffer et al.	
	6	20070158778		2007-07-12	Kitabatake et al.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT **(Not for submission under 37 CFR 1.99)**	Application Number		13415384
	Filing Date		2012-03-08
	First Named Inventor	Hebert	
	Art Unit		
	Examiner Name		
	Attorney Docket Number		125.288US02

	7	20070195563		2007-08-23	Shiraishi et al.	
	8	20070249092		2007-10-25	Joshi et al.	
	9	20080023785		2008-01-31	Hebert	
	10	20080023825		2008-01-31	Hebert et al.	
	11	20080024102		2008-01-31	Hebert et al.	
	12	20090039394		2009-02-12	UNO et al.	
	13	20090057869		2009-03-05	Hebert et al.	
	14	20090072368		2009-03-19	Hu et al.	
	15	20090263947		2009-10-22	Hebert	
	16	20100133644		2010-06-03	Hebert	
	17	20100140693		2010-06-10	Hebert	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Application Number	13415384
	Filing Date	2012-03-08
	First Named Inventor	Hebert
	Art Unit	
	Examiner Name	
	Attorney Docket Number	125.288US02

	18	20100155837		2010-06-24	Hebert	
	19	20100155915		2010-06-24	Bell et al.	

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FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number3	Country Code2 i	Kind Code4	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T5
	1							☐

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NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T5
	1		☐

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EXAMINER SIGNATURE

Examiner Signature		Date Considered	

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OR

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☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Jay Wahlquist/	Date (YYYY-MM-DD)	2012-03-16
Name/Print	Wahlquist, Jay A.	Registration Number	55705

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	12321807
Application Number:	13415384
International Application Number:	
Confirmation Number:	5259
Title of Invention:	SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD
First Named Inventor/Applicant Name:	Francois Hebert
Customer Number:	94108
Filer:	Jay Alan Wahlquist/Robert Thrumston
Filer Authorized By:	Jay Alan Wahlquist
Attorney Docket Number:	125.288US02
Receipt Date:	19-MAR-2012
Filing Date:	
Time Stamp:	09:25:52
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	00292551.PDF	987797 99152806049a46c2dcf3b6b14564c23bd0716616	no	6

Warnings:

Information:

Total Files Size (in bytes):	987797

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/81 (01-09)
Approved for use through 02/28/2011. OMB 0651-0035
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

POWER OF ATTORNEY OR REVOCATION OF POWER OF ATTORNEY WITH A NEW POWER OF ATTORNEY AND CHANGE OF CORRESPONDENCE ADDRESS

Application Number	12/471,911
Filing Date	5/26/2009
First Named Inventor	Hebert
Title	SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD
Art Unit	
Examiner Name	
Attorney Docket Number	125.288US01

I hereby revoke all previous powers of attorney given in the above-identified application.

☐ A Power of Attorney is submitted herewith.

OR

☒ I hereby appoint Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith: 94108

OR

☐ I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

Practitioner(s) Name	Registration Number

Please recognize or change the correspondence address for the above-identified application to:

☒ The address associated with the above-mentioned Customer Number:

OR

☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the:

☐ Applicant/Inventor

☒ Assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) (Form PTO/SB/96) submitted herewith or filed on __________.

SIGNATURE of Applicant or Assignee of Record

Signature	Paul Bernkopf	Date	12/7/2010
Name	Paul Bernkopf	Telephone	321-724-7557
Title and Company	Chief Intellectual Property Counsel INTERSIL AMERICAS INC.		

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of ________ forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

PTO/SB/96 (10-07)
Approved for use through 10/31/2007. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Intersil Americas Inc.

Application No./Patent No.: 12/471,911 Filed/Issue Date: May 26, 2009

Entitled: SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD
(Attorney Docket No. SE-2603-TD / 125.288US01)

Intersil Americas Inc. (Name of Assignee), a Corporation (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.),

states that it is:

1. ☒ the assignee of the entire right, title, and interest; or
2. ☐ an assignee of less than the entire right, title and interest.
   The extent (by percentage) of its ownership interest is _________ %

In the patent application/patent identified above by virtue of either:

A. ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 022734, Frame 0065, or for which a copy thereof is attached.

OR

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From:_______________ To:_______________
   The document was recorded in the United States Patent and Trademark Office at
   Reel ___________, Frame ___________, or for which a copy thereof is attached.
2. From:_______________ To:_______________
   The document was recorded in the United States Patent and Trademark Office at
   Reel ___________, Frame ___________, or for which a copy thereof is attached.
3. From:_______________ To:_______________
   The document was recorded in the United States Patent and Trademark Office at
   Reel ___________, Frame ___________, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet.

☒ As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.
[NOTE: A separate copy (*i.e.,* a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Paul Bernkopf
Signature

12/7/2010
Date

Paul Bernkopf
Printed or Typed Name

321-724-7557
Telephone Number

Chief Intellectual Property Counsel
Title

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD
First Named Inventor/Applicant Name:	Francois Hebert
Filer:	Jay Alan Wahlquist/Jennifer Swanson
Attorney Docket Number:	125.288US02

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	380	380
Utility Search Fee	1111	1	620	620
Utility Examination Fee	1311	1	250	250
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1250**

Electronic Acknowledgement Receipt

EFS ID:	12246724
Application Number:	13415384
International Application Number:	
Confirmation Number:	5259
Title of Invention:	SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD
First Named Inventor/Applicant Name:	Francois Hebert
Customer Number:	94108
Filer:	Jay Alan Wahlquist/Jennifer Swanson
Filer Authorized By:	Jay Alan Wahlquist
Attorney Docket Number:	125.288US02
Receipt Date:	08-MAR-2012
Filing Date:	
Time Stamp:	16:18:44
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$1250
RAM confirmation Number	3071
Deposit Account	502432
Authorized User	FOGG,DAVID N.

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	00290842.PDF	1223267 de899f6114d31010923ecf5937aece346c804195	no	4
Warnings:					
Information:					
2	Oath or Declaration filed	00290751.PDF	149249 13d9bd0ffec99d4553fbd0571129b61c905351af	no	3
Warnings:					
Information:					
3	Drawings-only black and white line drawings	00290747.PDF	319421 c2bd5c1d90762a338b04dd6d3fe833d2fb61a57b	no	8
Warnings:					
Information:					
4		00290968.PDF	126041 90a5050e09bc28925b6da5393f29cb873ae5e1bf	yes	28

Multipart Description/PDF files in .zip description

Document Description	Start	End
Specification	1	20
Claims	21	27
Abstract	28	28

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
Warnings:					
Information:					
5	Power of Attorney	00291182.PDF	80698 8a213d250b96b30dfd10c04fede28ddfd3b3820d	no	1
Warnings:					
Information:					
6	Assignee showing of ownership per 37 CFR 3.73(b).	00291180.PDF	74877 a7b378c4a58f67a9bb2b3bcabced5f89f6ce16a3	no	1
Warnings:					

Information:					
7	Fee Worksheet (SB06)	fee-info.pdf	33311 14c924bd948deaad91ae994d9a3249cb83cf13f8	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	2006864		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	125.288US02
	Application Number	

Title of Invention	SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Applicant Information:

Applicant 1 Remove

Applicant Authority ● Inventor ○ Legal Representative under 35 U.S.C. 117 ○ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Francois		Hebert	

Residence Information (Select One) ● US Residency ○ Non US Residency ○ Active US Military Service

City	San Mateo	**State/Province**	CA	**Country of Residence** i	US

Citizenship under 37 CFR 1.41(b) i	CA

Mailing Address of Applicant:

Address 1	18 Melrose Court		
Address 2			
City	San Mateo	**State/Province**	CA
Postal Code	94402	**Country**i	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	94108
Email Address	Add Email Remove Email

Application Information:

Title of the Invention	SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD		
Attorney Docket Number	125.288US02	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		**Sub Class (if any)**	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	8	**Suggested Figure for Publication (if any)**	

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	125.288US02
	Application Number	

Title of Invention	SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S. C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Enter either Customer Number or complete the Representative Name section below. If both sections are completed the Customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	94108		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation of	12/471,911	2009-05-26
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
12471911	non provisional of	61162232	2009-03-20
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
12471911	non provisional of	61140610	2008-12-23
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.			Add

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).

			Remove
Application Number	Country i	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
			● Yes ○ No

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	125.288US02
	Application Number	

Title of Invention	SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Assignee Information:

Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office.

Assignee 1 Remove

If the Assignee is an Organization check here. ☒

Organization Name	Intersil Americas Inc.		
Mailing Address Information:			
Address 1	1001 Murphy Ranch Road		
Address 2			
City	Milpitas	**State/Province**	CA
Country i	US	Postal Code	95035
Phone Number		Fax Number	
Email Address			

Additional Assignee Data may be generated within this form by selecting the **Add** button. Add

Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.

Signature	/Jay Wahlquist/			Date (YYYY-MM-DD)	2012-03-07
First Name	Jay	Last Name	Wahlquist	Registration Number	55705

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ATTORNEY DOCKET NO.: 0008.0014
CLIENT REF. NO.: SE-2603-TD

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD

the specification of which: ☒ is attached hereto.
☐ was filed on: ____________
as United States Application No.: ____________
or PCT International Application No.: ____________
and was amended on: ____________ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 C.F.R. § 1.56.

Prior Foreign Application(s)

I hereby claim foreign priority benefits under 35 U.S.C. §§ 119(a)-(d) or (f), or § 365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or § 365(a) of any PCT international application(s) designating at least one country other than the United States of America, listed below and have also identified below by checking the box, any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or any PCT international application(s) having a filing date before that of the application(s) of which priority is claimed:

Application Number	Country	Date of Filing (day, month, year)	Date of Issue (day, month, year)	Priority Claimed	
				Yes ☐	No ☐
				Yes ☐	No ☐
				Yes ☐	No ☐

Authorization to Permit Access to Application by Participating Offices

☒ If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), and any other intellectual property offices in which a foreign application claiming priority to the above-identified patent application is filed access to the above-identified patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, or other intellectual property office in which a foreign application claiming priority to the above-identified application is filed to have access to the application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the application-as-filed with respect to: 1) the above-identified application, 2) any foreign application to which the above-identified application claims priority under 35 USC 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the above-identified US application, and 3) any U.S. application from which benefit is sought in the above-identified application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing the Authorization to Permit Access to Application by Participating Offices.

Prior Provisional Application(s)

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below:

Application Number	Date of Filing (day, month, year)
61/140,610	23 December, 2008
61/162,232	20 March, 2009

Prior United States Application(s)

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s), or § 365(c) of any PCT international application(s) designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application(s) in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose information material to patentability as defined in 37 C.F.R. § 1.56 which became available between the filing date of the prior application(s) and the national or PCT international filing date of this application:

Application Number	Date of Filing (day, month, year)	Status - Patented, Pending, Abandoned

And I hereby appoint, both jointly and severally, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith the MH2 Technology Law Group LLP attorneys and agents associated with:

CUSTOMER NUMBER
39878

All correspondence and telephone communications should be addressed to:

CUSTOMER NUMBER
39878

corresponding to the law firm of MH2 Technology Law Group LLP, 1951 Kidwell Drive, Suite 550, Tysons Corner, VA 22182; telephone number (703) 917-0000; facsimile number (703) 997-4905.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine and imprisonment, or both, under 18 U.S.C. § 1001, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

NAME OF SOLE OR FIRST INVENTOR: ☐ A petition has been filed for this unsigned inventor

Signature Francois Hebert Date May 22, 2009

Given Name (first and middle (if any)) **Francois** Family Name or Surname **HEBERT**

Citizenship: Canada

Residence: 18 Melrose Court, San Mateo, CA 94402

Mailing Address: 18 Melrose Court, San Mateo, CA 94402

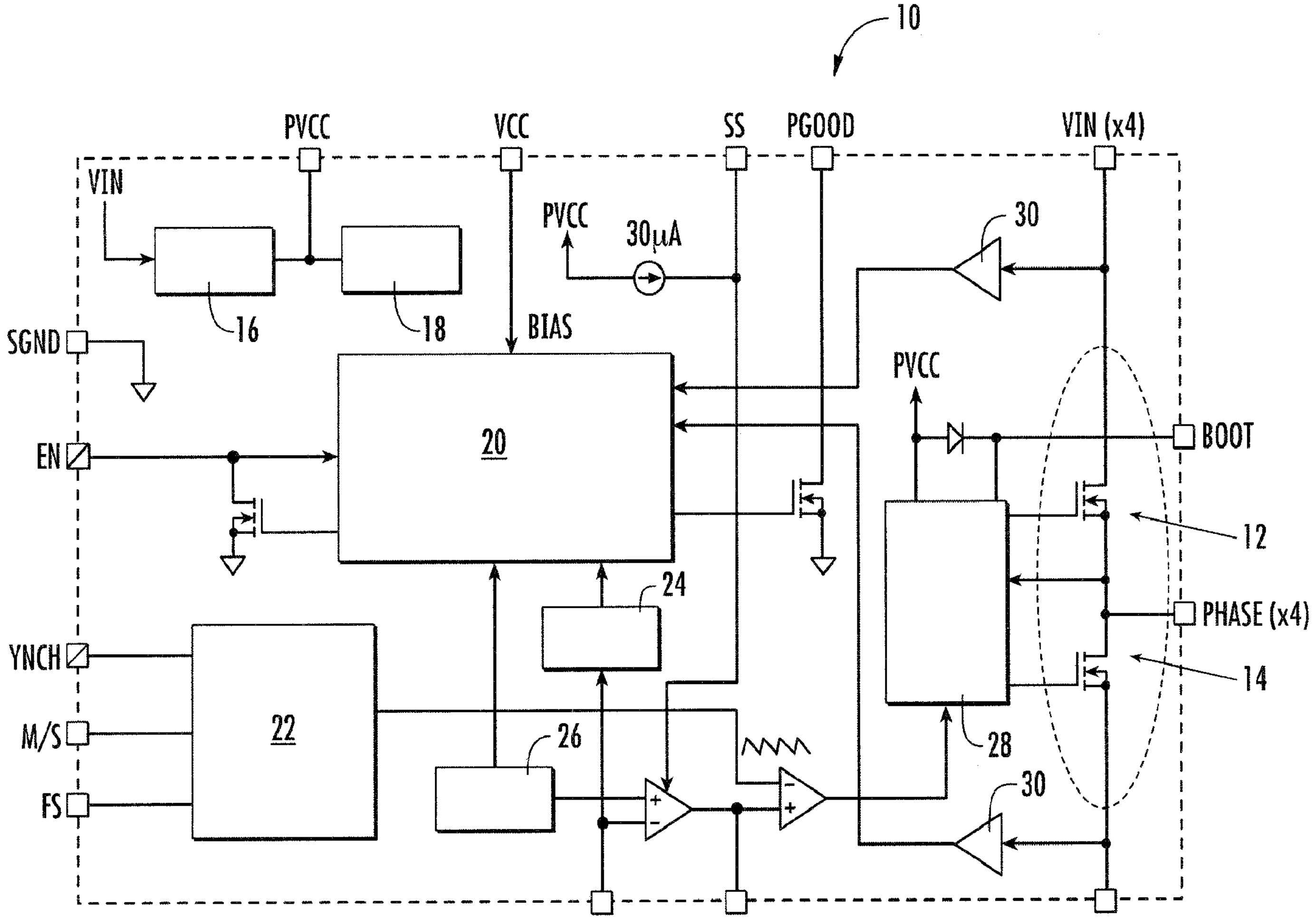
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FIG. 1

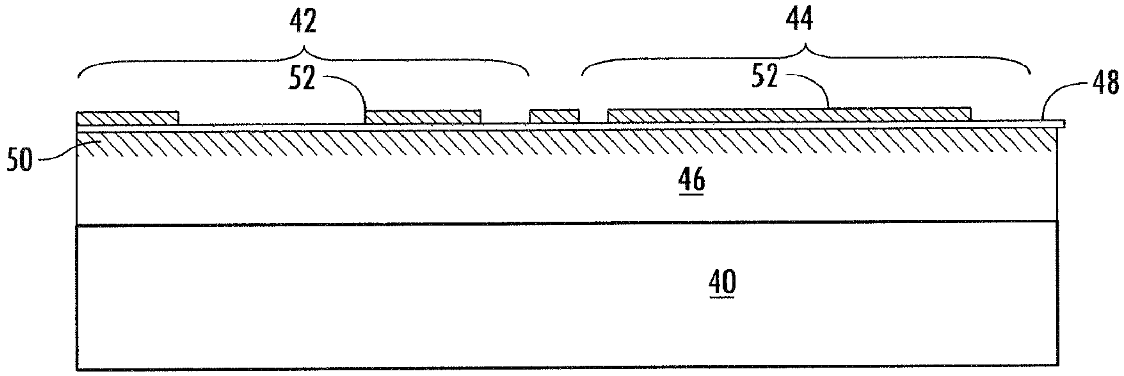


FIG. 2

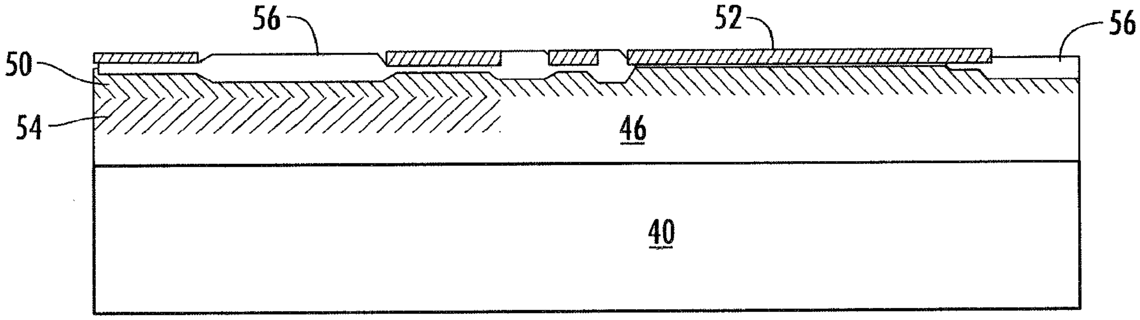


FIG. 3

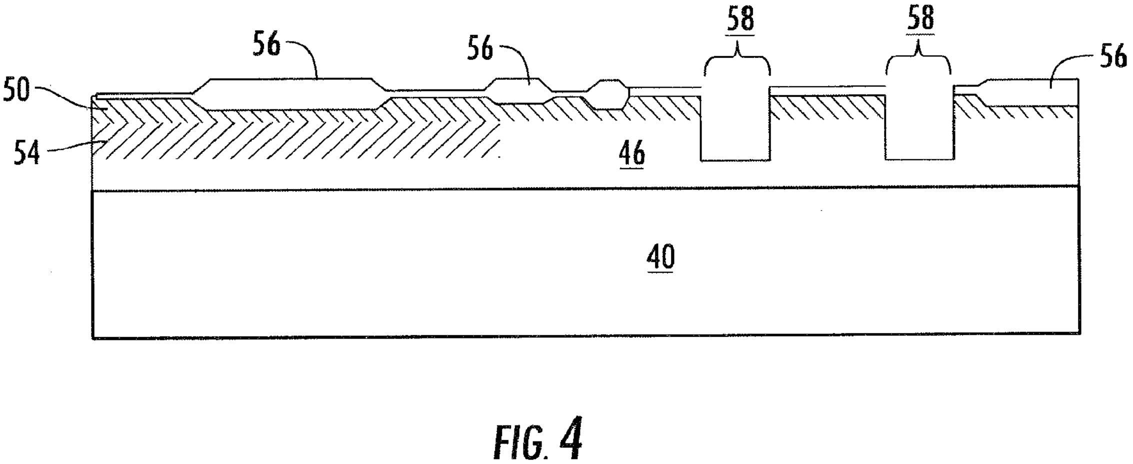


FIG. 4

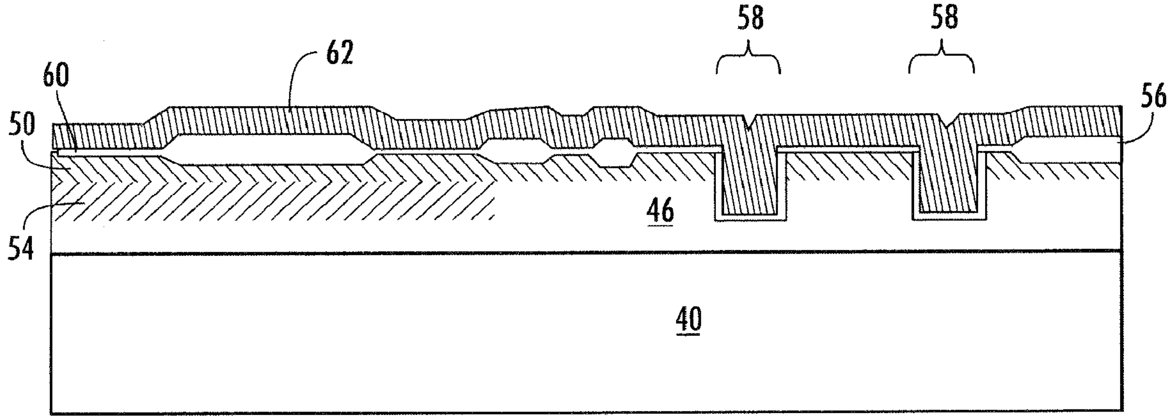


FIG. 5

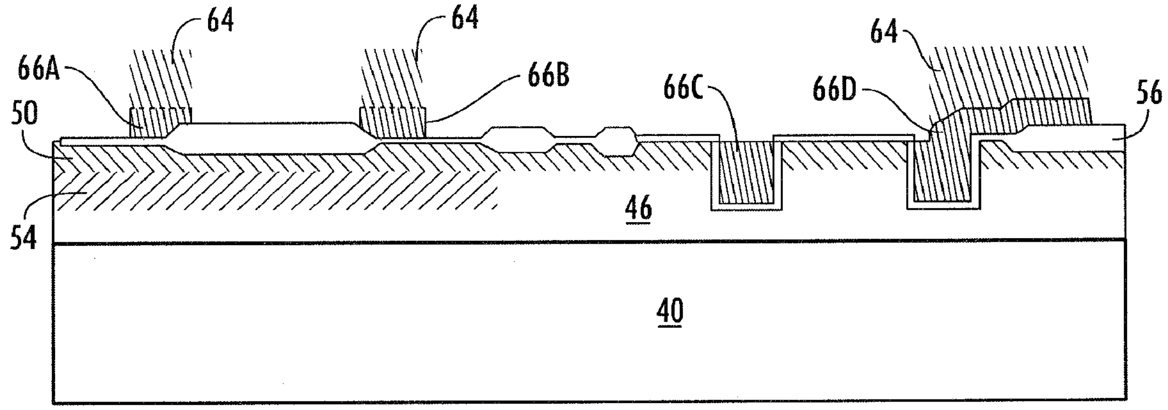


FIG. 6

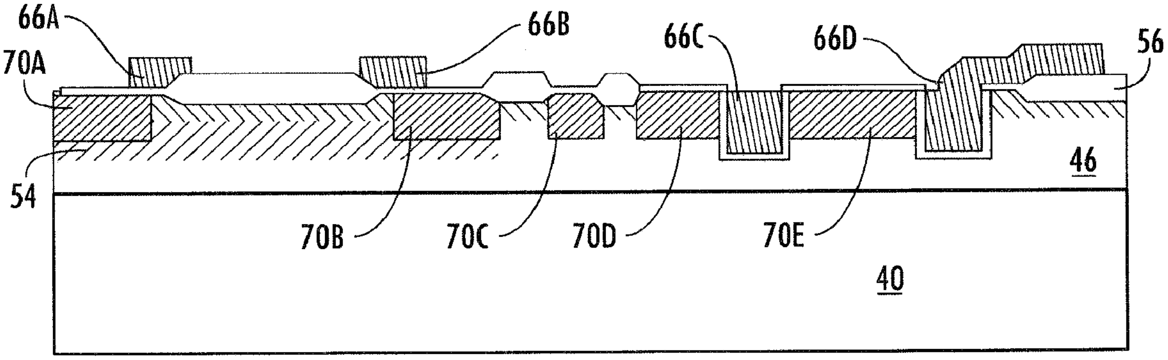


FIG. 7

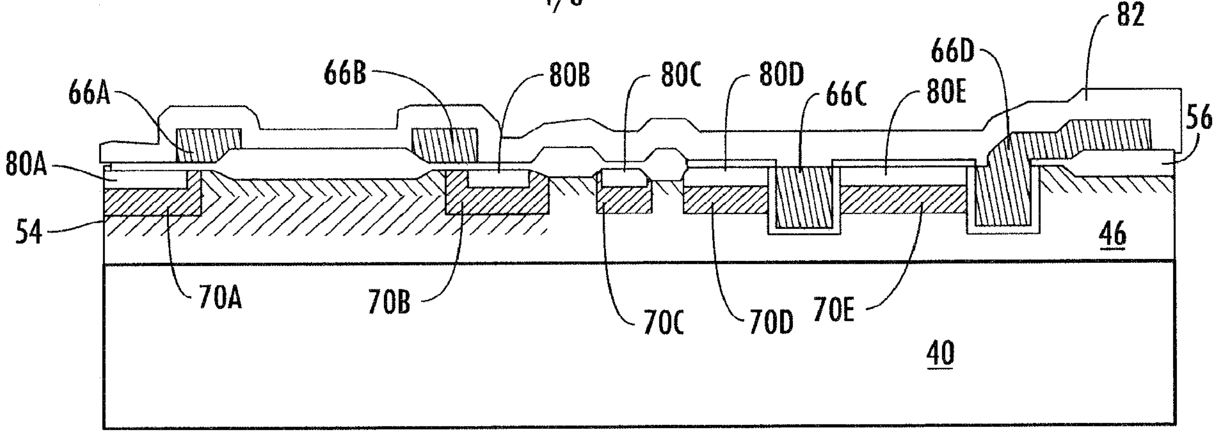


FIG. 8

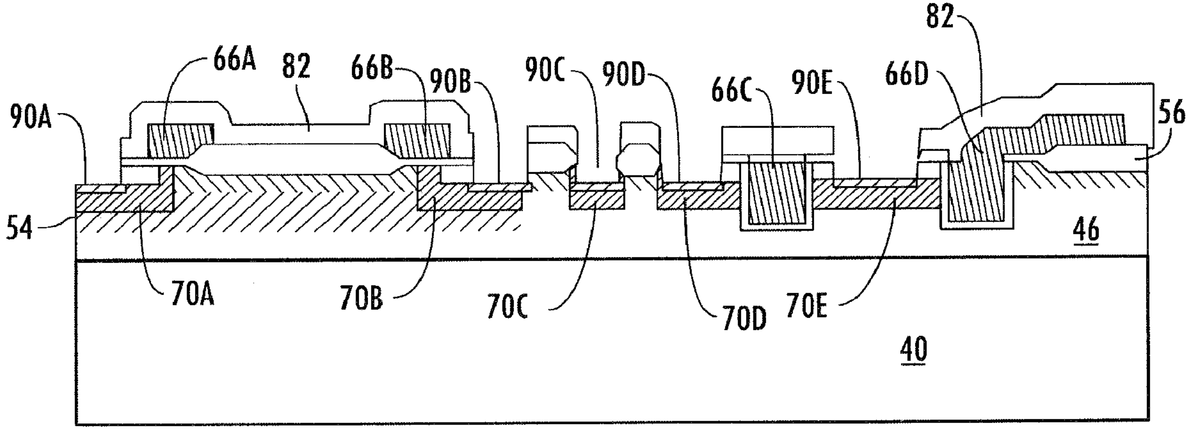


FIG. 9

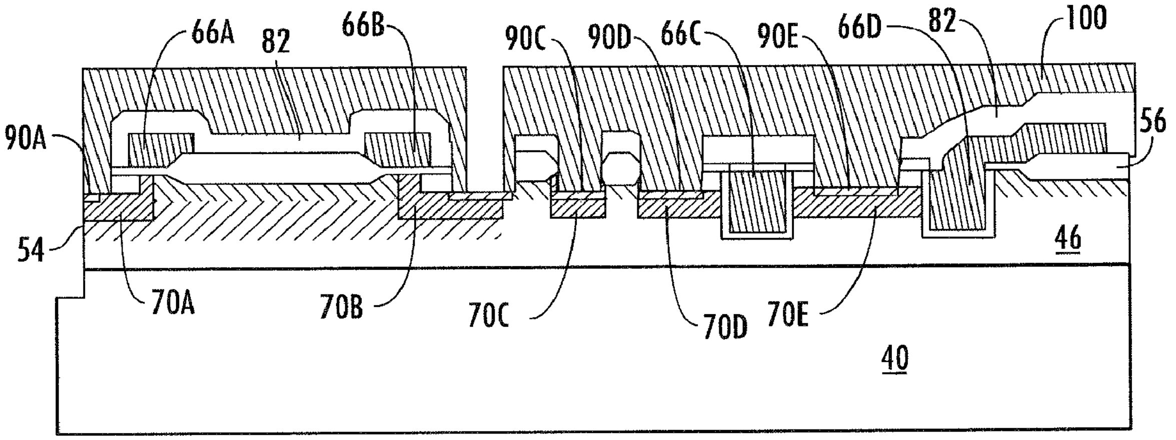


FIG. 10

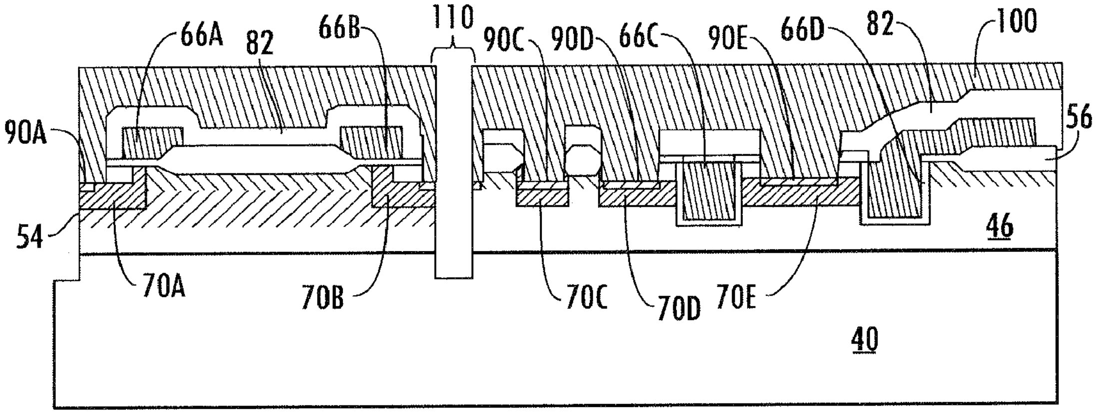


FIG. 11

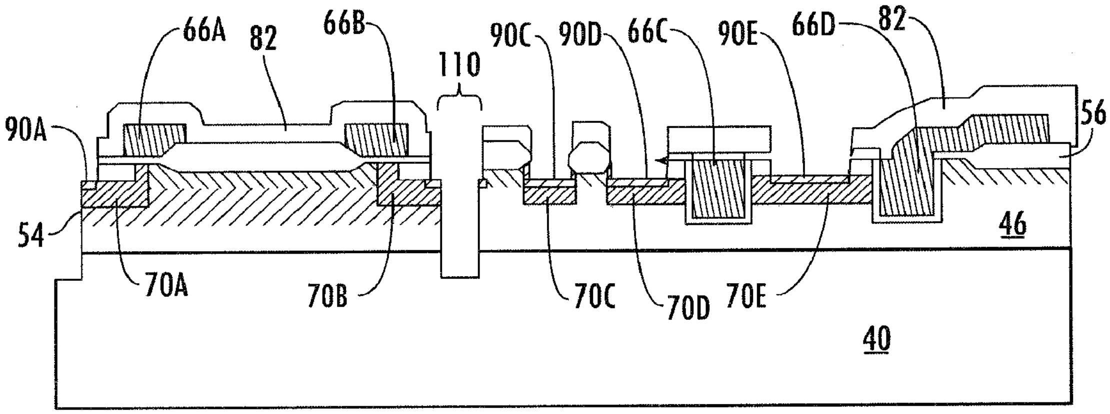


FIG. 12

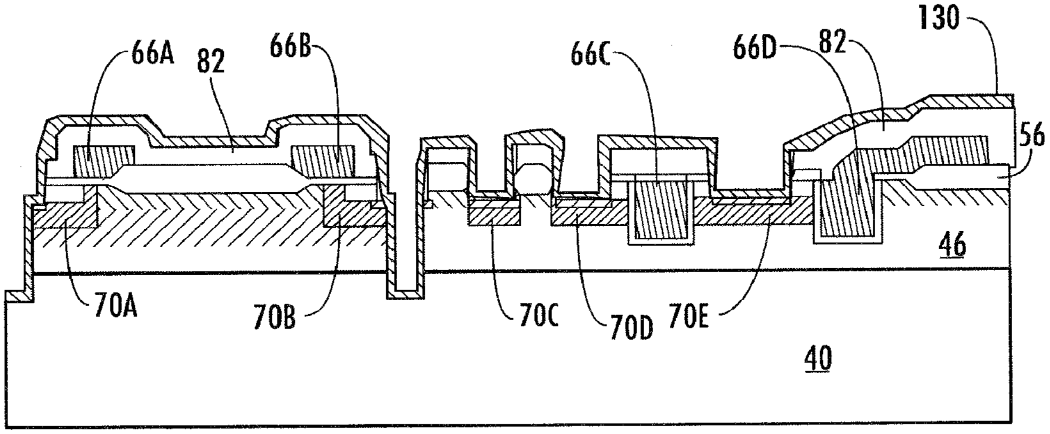


FIG. 13

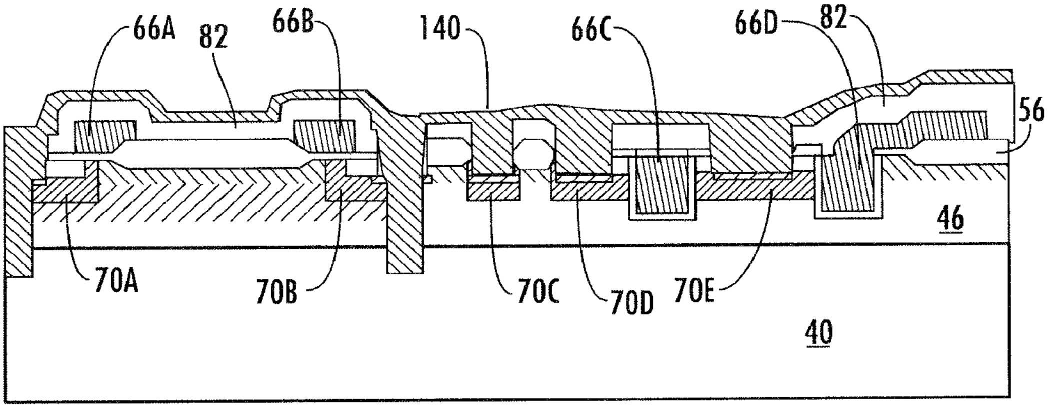


FIG. 14

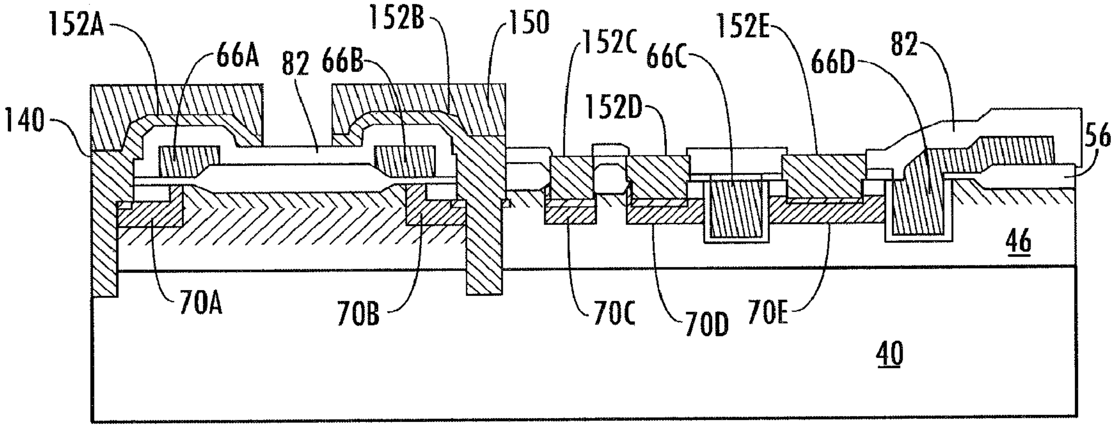


FIG. 15

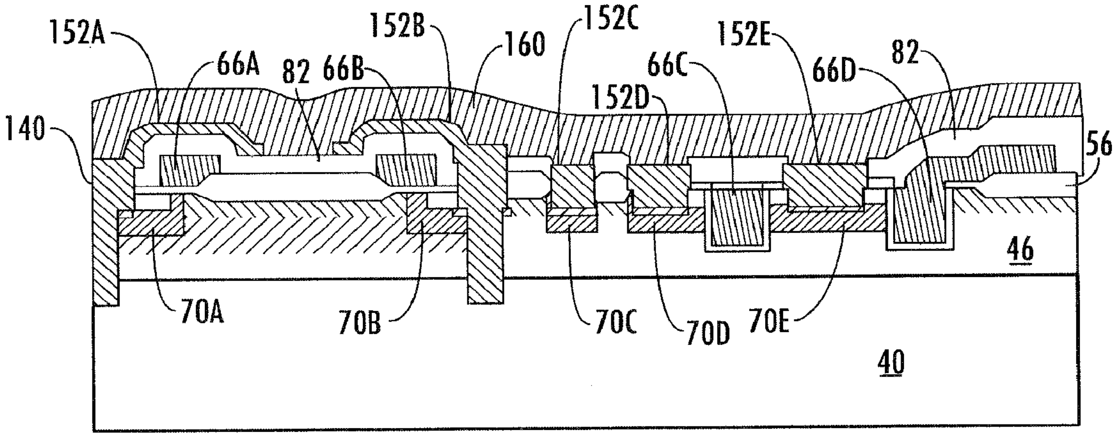
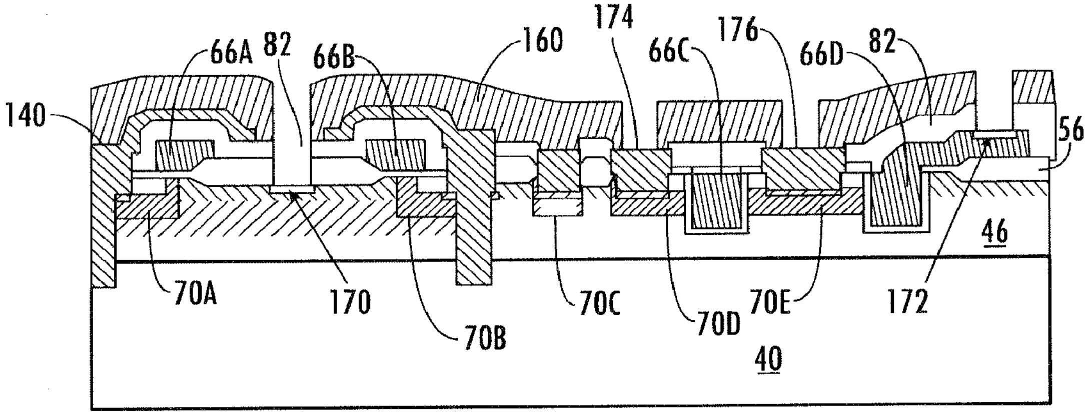


FIG. 16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70E
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40

FIG. 17

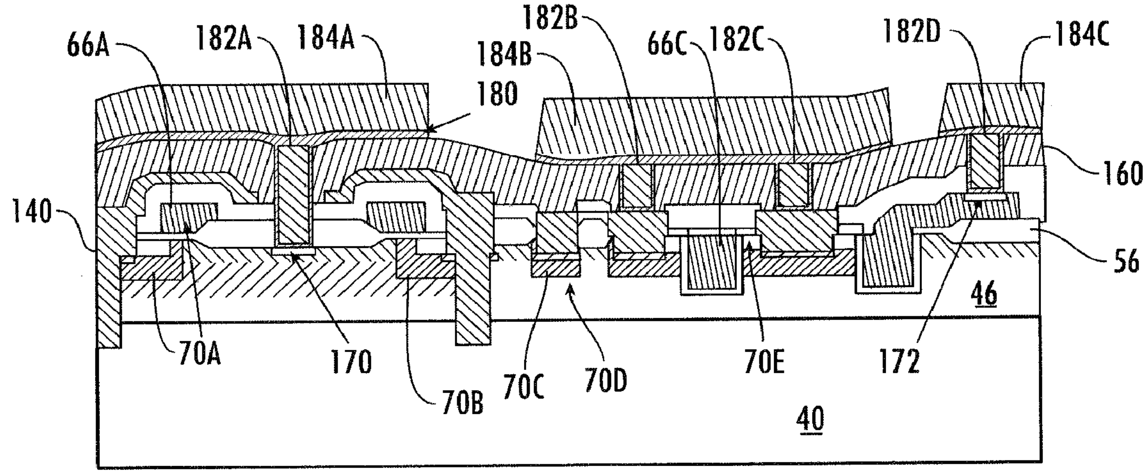
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FIG. 18

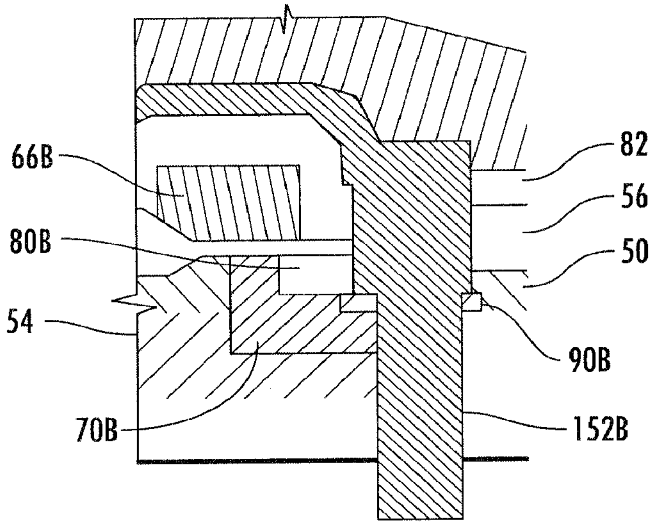

FIG. 19

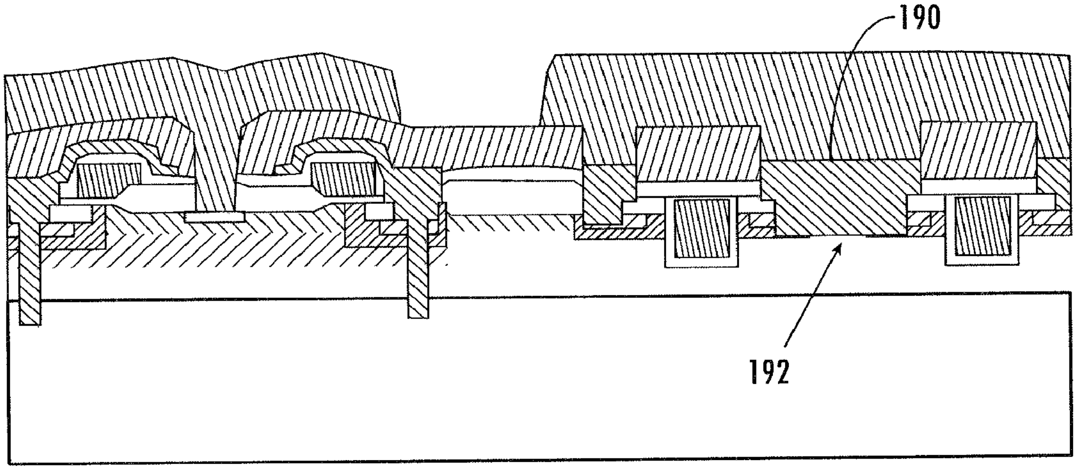

FIG. 20

SINGLE DIE OUTPUT POWER STAGE USING TRENCH-GATE LOW-SIDE AND LDMOS HIGH-SIDE MOSFETS, STRUCTURE AND METHOD

Cross-Reference to Related Application

[0001] This application is a continuation of U.S. Patent Application Serial No. 12/471,911, filed May 26, 2009, which claims the benefit of provisional U.S. Provisional Application No. 61/140,610, filed December 23, 2008, and U.S. Provisional Application No. 61/162,232, filed March 20, 2009.

Field of the Invention

[0002] This invention relates to the field of semiconductor devices, and more particularly to power conversion and control structures and their methods of formation.

Background of the Invention

[0003] Semiconductor devices which provide power converter functionality, for example for altering DC power using a DC to DC (DC-DC) converter, are used in various capacities. For example, input DC power from one or more batteries can be converted to provide one or more power outputs at voltages which can be higher or lower than the input DC voltage. Performing a power conversion function using integrated circuits (IC's) typically requires a control circuit, a DC high-side device electrically coupled with voltage in (V_{IN}), and a DC low-side device electrically coupled with ground. In a synchronous step-down device (i.e. a "synch buck" converter), for example, power conversion is performed to decrease voltage by alternately enabling the high-side device and the low-side device, with a switching and control function being performed by the controller circuit with high efficiency and low power loss through the device.

[0004] Power converter circuits which can operate at a high power density (for example, high voltage and high current) are needed, particularly devices which can efficiently convert high density power at a reasonable cost. One challenge with high power density is that the size of the output circuitry increases as the voltage and current rating of the converter increases. Different implementations of the controller circuit, the high-side device, and the low-side device have been used, each with its own advantages and disadvantages.

[0005] Monolithic devices could be formed which contain the controller circuit, the high-side device, and the low-side device on a single piece of silicon. In high density devices, the percent of silicon containing the controller circuitry is much smaller than the percent of silicon containing the high current output devices. The output power devices can require more than 50% of the die surface. However, forming the controller circuitry can require providing CMOS devices, bipolar devices, LDMOS devices, nonvolatile memory, diodes, resistors, capacitors, etc., and can involve the use of more than 20 mask steps during the fabrication process. In contrast, forming the output power devices can require eight or fewer mask steps for their fabrication. Because of mask misalignment and other processing issues, processing failures increase with increasing mask steps. Thus forming the controller circuitry and output devices on the same piece of silicon is inefficient and costly, because silicon formed with an eight mask process is subject to a 20 mask process failure rate and extra cost (equivalent to 12 extra mask layers). As such, monolithic devices are not used to integrate the power devices with the controller circuitry.

[0006] Co-packaged devices can include controller circuitry on one semiconductor die, the high-side device on a second die, and the low-side device on a third die. In one type of co-packaged device, the controller circuitry on one die is then connected to the high-side and low-side devices formed from standard vertical MOSFETs on the other two dies using bond wires or other connections. In another type of device, the controller circuitry on one die is the connected to the high-side device including bottom-source lateral diffusion metal oxide semiconductor (LDMOS) and a low-side vertical diffusion MOS (DMOS) device. In both of these devices, the three separate dies are then encapsulated or otherwise packaged together in one IC device. Forming controller, low-side, and high-side devices on separate dies overcomes the above-stated problems of monolithic devices. However, co-packaged devices can have problems with interconnection parasitics on the controller IC which can negatively influence device performance. This may result from parasitic inductance inherent in bond wires, electromagnetic interference (EMI), ringing, efficiency loss, etc. Higher-quality connections such as copper plate (or clip) bonding, or ribbon bonding, can be used to reduce parasitics, but this increases assembly costs. Further, co-packaging standard vertical MOSFETs can result in a circuit with parasitic inductance in series with the output node. Problems caused by parasitic inductances are well established in the art. While a capacitor can be connected to the output terminals such as the input (V_{IN}) and ground, to compensate for the negative impact of inductances connected to these nodes, capacitances cannot be connected to internal nodes such as the Output (V_{OUT}, also referred to as phase node or switched node).

[0007] Additionally, packages containing three separate dies have higher production costs, for example because of the large number of die attach steps (three in this example), and additional space is required for spacing between adjacent dies to allow for die attach fillets, die placement tolerance, and die rotation tolerance, which reduces the power-density which can be achieved. Examples of co-packaged devices include non-synch buck with co-packaged high-side MOSFET and external Schottky diode, non-synch buck with co-packaged high-side and low-side

MOSFETs, synchronous buck with co-packaged high-side and low-side MOSFETs, boost converter with co-packaged MOSFET, and boost converter with co-packaged MOSFET and Schottky diodes.

[0008] Discrete devices can also be mounted separately to a printed circuit board. In this solution, a first packaged die containing controller circuitry is used in conjunction with a second packaged die containing a high-side MOSFET and a third package containing a low-side MOSFET. The three packages are mounted on a printed circuit board. However, this can increase packaging costs as the number of dies and separate packages which must be manufactured and handled is at least tripled, and the area used on the printed circuit board is also increased, leading to increased circuit board size.

[0009] There is a need for power converters in which device processing costs are reduced while providing a power converter device which has sufficient device electrical characteristics with low parasitic inductance and capacitance.

[0010] Co-pending U.S. Pat. Application Serial No. 12/470,229 titled "Co-Packaging Approach for Power Converters Based on Planar Devices, Structure and Method", having the same inventor and assignee as the present application and incorporated herein by reference in its entirety, describes a structure for providing voltage converter power devices (high-side and low-side output devices) on a single die. A structure includes the use of a lateral diffusion MOS (LDMOS) device as a high-side device and a planar vertical diffusion MOS (VDMOS) device as the low-side device. While providing reasonable cost and manufacturability which is sufficient for many uses, a low-side planar VDMOS device may not achieve a minimum specific resistance (RDS*Area) in other uses, for example because the transistor channel is planar, the cell pitch is relatively large, and there is a parasitic junction field effect transistor (JFET) resistance between adjacent body diffusions.

Brief Description of the Drawings

[0011] The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description, serve to explain the principles of the invention. In the figures:

[0012] FIG. 1 is an electrical schematic including a voltage converter device;

[0013] FIGS. 2-19 are cross sections depicting a first embodiment of a method and intervening structures of a voltage converter output structure; and

[0014] FIG. 20 is a cross section depicting a second embodiment of a voltage converter output structure.

[0015] It should be noted that some details of the FIGS. have been simplified and are drawn to facilitate understanding of the inventive embodiments rather than to maintain strict structural accuracy, detail, and scale.

Description of the Embodiments

[0016] Reference will now be made in detail to the present embodiments (exemplary embodiments) of the invention, an examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

[0017] There is a need for power converters which are suited for very high current applications which have an RDS_{ON} in the milliohm range, and which can be optimized based on the circuit requirements. In particular, a device which allows formation of high-side and low-side power converter output devices on a single die of minimum size to reduce costs, which includes a low resistance low-side device, and which provides a power converter device which has sufficient device electrical characteristics for high-frequency of operation at high power densities (high voltage and high current) with low parasitic inductance and capacitance would be desirable.

[0018] In an embodiment of the device, the high-side and low-side devices can be combined monolithically on one substrate (a first die, a "PowerDie"), with one substrate (a second die) for the control circuitry. The high-side device can be formed using a high performance lateral N-channel diffusion metal oxide semiconductor (LDMOS) field effect transistor (FET), and the low-side device can be formed from an N-channel vertical diffusion metal oxide semiconductor (DMOS) FET having a trench-gate. A low-side vertical diffusion MOSFET using a trench-gate can achieve an on-resistance (R_{SP}) which is one-half or less of a planar-gate VDMOS device with the same breakdown voltage. This, at least in part, can result from a smaller cell pitch and because there is no parasitic JFET in the trench-gate VDMOS.

[0019] One difficulty in combining a low-side trench-gate VDMOS and a high-side planar-gate LDMOS is that a complex process with many mask steps can result. A planar-gate LDMOS device uses a surface (hence planar) channel, diffused from the source side of the gate, laterally under the planar gate. If a trench-gate VDMOS is used as the low-side device, the channel of this device is along the sidewalls of a gate trench, formed by a body diffusion from the top surface into the silicon. Using standard processing techniques, if possible, would result in at least separate body masking, a body implant, and a body diffusion to form each device.

[0020] An embodiment of the invention thus includes a first die having output power devices and a second die having a controller circuit. The first die can include a novel high-side planar-gate LDMOS device with a low-side trench-gate DMOS, with or without an integrated Schottky diode across the body to drain junction, formed using a low number of processing stages. Trench-gate VDMOS structures are proposed for high-current applications in the low-side device because of their lower R_{DS}*Area figure of merit, which can result from the absence of JFET parasitic resistance, at least partially resulting from a vertical channel and a smaller cell pitch.

[0021] FIG. 1 depicts a circuit block diagram of a circuit 10 including a power converter. Depicted are output devices including a high-side device 12 and a low side device 14. This device schematic depicts a pair of N-channel MOSFET enhancement mode devices for use as the output devices. In an embodiment of the inventive device, an LDMOS MOSFET is used as the high-side device and a planar vertical DMOS MOSFET as the low-side device in a voltage converter circuit.

[0022] In addition to the signals and connections depicted, the voltage converter of FIG. 1 can include the following: series regulator 16; POR monitor 18; fault monitoring 20; clock and oscillator generator 22; voltage monitor 24; 0.6V reference 26; gate drive and adaptive shoot thru protection 28; OC monitors 30.

[0023] In the description of the embodiments below, it will be understood by those of ordinary skill in the art that the description is exemplary. Variations to the processes and resulting structures of the various embodiments, for example to the materials, thicknesses and widths, doping concentrations, etc., will be apparent. Also, some additional processing stages and material/doping layers can be included in the described processes, while other described structures and process stages may be optional and not required to form a functional device. Further, the drawings depict power devices with "striped" gate fingers, which are parallel. Variations of the geometries are possible, such as "closed cell" geometries which are well known by those of ordinary skill in the art of power devices. A closed cell geometry refers to structures with gate fingers which surround the source and body contact. The cells can be square, rectangular, hexagonal, etc.

[0024] FIG. 2 depicts a substrate 40 which can include a wafer or wafer portion of a material including, for example, silicon, gallium arsenide, gallium nitride, silicon carbide. A high-side output power device will be formed at a first wafer location 42, and a low-side output power device will be formed at a second wafer location 44. The substrate 40 can be heavily doped to an N-type conductivity (N+++), for example with arsenic to a concentration of about 1E18 to 1E20 atoms/cm^3. In another embodiment, the substrate 40 can be a red-phosphorous doped substrate, which would reduce the overall RDS_{ON} of the device. The semiconductor substrate is (or will subsequently be) configured such that the depicted region will provide its output to the power converter inductor to provide a device switched node. An N-type epitaxial (epi) layer 46 can formed according to techniques known in the art on the silicon substrate to a thickness which is a function of the desired breakdown voltage of the vertical low-side device to be formed in region 44. For a 30V breakdown voltage for example, the thickness may be in the range of about 2.5 microns to about 5 microns thick, with a doping concentration in the range of between about 2E16 atoms/cm^3 to about 3E16 atoms/cm^3. For lower-operating voltages, the epitaxial layer thickness would be reduced (as thin as 0.5 micron for example), and the epitaxial doping concentration would be increased (up to 5E16 for example). For higher operating voltages, the epi thickness would be increased and the doping concentration would be reduced. A pad dielectric (pad oxide) 47 to reduce stress, protect the substrate surface, and screen contaminants from any subsequent ion implantation step can be formed to a thickness of between about 150 angstroms (Å) to about 400 Å on the epi layer. If a red-phosphorous substrate is used, the thickness of the N- epitaxial layer can be increased to compensate for the higher up-diffusion of phosphorous from the substrate. For example, in an arsenic-doped substrate for use with a 30V device, an N-epitaxial layer can be about 3 μm nominal thickness. In an equivalent red-phosphorous doped substrate, the N-epitaxial layer can have a thickness of between about 4.5 μm to about 6 μm. Next, a blanket N-type drift implant 50 can be performed to provide, for example, a high-side LDMOS drain region, using a dose of phosphorous in the range of about 5E11 to about 4E13 atoms/cm^2 at an implant energy of between about 40 KeV to about 360KeV. A oxidation masking layer 52 such as a patterned nitride layer can be formed to result in a structure similar to FIG. 2.

[0025] Next, a patterned deep body P-type (for example, boron) implant can be performed using a photoresist (resist) mask. The implant can be performed at an energy of between about 1 MeV to about 2 MeV and a dose of between about 1E13 atoms/cm^2 and about 1E14 atoms/cm^2 to provide deep body implant region 54 in the high-side device region 42. A relatively thick resist mask can be used, for example in the range of between about 4 microns to about 5 microns, to reliably block an implant performed at an energy of $\geq$1 MeV. The resist mask can be stripped, then a wafer clean can be performed. Next, the deep body implanted boron can be diffused to a sufficient depth by performing an anneal at a temperature of between about 1,050°C and about 1,200°C for between about 20 minutes to about 5 hours using an oxygen bleed during the beginning of this anneal, followed by a nitrogen ambient. Subsequently, a field oxidation can be performed to result in field oxide 56, then the nitride 52 can be stripped.

[0026] Next, a patterned trench-gate mask (not depicted) is formed to leave low-side trench-gate regions of the substrate exposed. An oxide etch to remove native or other oxide, then a silicon etch is performed to form trench-gate openings 58 in the substrate. One or more optional trench-sidewall implants can be performed which can adjust a threshold voltage (V_T) of the completed low-side device. Tilted implants with wafer rotation can be performed. The implants can include phosphorous to lower V_T or boron to raise V_T. An energy of between about 20 KeV and about 80 KeV at a wafer tilt of between about 4° and about 12° would be sufficient. An optional gate-trench bottom implant can be performed using an N-type dopant to increase conductivity or a P-type dopant to reduce net concentration and C_{GD} would be sufficient. The trench-gate mask is removed to form a structure similar to FIG. 4.

[0027] A sacrificial oxidation (sac ox) followed by a sac ox strip can be performed to remove any damaged portions of the epitaxial silicon layer 46. A gate oxidation can be performed to form gate oxide 60, then a gate polysilicon deposition and doping and/or a polycide deposition can be performed to result in blanket transistor gate layer 62 as depicted in FIG. 5. The polysilicon can be doped by ion implantation, diffusion ($POCl_3$, for example), or *in situ* doped during deposition. An optional silicide layer, for example WSi_x, can be added over the gate polysilicon layer to reduce resistance. An optional capping layer can also be formed over the transistor gate layer 62.

[0028] As depicted in FIG. 6, a patterned resist layer gate mask 64 can be formed over the blanket gate layer, then the gate layer is etched to result a structure similar to that depicted including transistor gate portions 66A-66D. The gate layer can be over-etched to recess the gate material within the gate trenches. The polysilicon portion 66C is self-aligned within the trench. Gate portions 66A and 66B will form a gate of the high-side LDMOS device, and gate portions 66C, 66D will form portions of a gate for one of the active cells of the low-side trench-gate MOSFET device. Gate portion 66D will form the gate to the active cell where the polysilicon is recessed below the epitaxial layer surface, as well as an electrode to enable connection of the polysilicon layer to a subsequently formed metal layer above the epitaxial layer surface and away from the gate trenches. Thus these functions are performed using different parts of a single conductive structure, which can include one or more conductive layers.

[0029] Next, the resist 64 can be removed then an unmasked (blanket) body implant of the FIG. 6 structure can be performed to result in a structure similar to FIG. 7 including body regions 70A-70E. This implant is self-aligned as no separate mask is needed, because the gate polysilicon and field oxide provide a sufficient mask. An implant of boron to a dose of between about 5E12 atoms/cm^2 and about 5E14 atoms/cm^2 at an energy of between about 20 KeV to about 80 KeV using no tilt would be sufficient. To diffuse the boron under the gates, a body (channel) drive anneal at a temperature of between about 1,000°C and about 1,150°C for a duration of between about 20 minutes to 3 hours in a nitrogen (N_2) ambient would provide a sufficient body diffusion.

[0030] Advantageously, the same body diffusion region for both the high-side region 42 and the low-side region 44 can be used because the same gate oxide and same background doping is used for both devices. This can eliminate the need for a separate mask step to form each device and decrease other associated processing requirements, thereby reducing costs over conventional processes.

[0031] A blanket source implant can then be performed, for example using arsenic at a dose of between about 4E15 atoms/cm^2 and about 10E15 atoms/cm^2. This blanket source implant is also sufficiently blocked by the gate polysilicon and the field oxide, and is therefore self-aligned to form source implant regions 80A-80E. An oxide deposition is performed to a thickness of between about 1,500 Å and about 3,500 Å, for example to about 2,500 Å. A source anneal at a temperature of between about 900°C and about 1,000°C in oxygen would sufficiently densify the oxide to result in blanket oxide layer 82.

[0032] Next, a patterned body contact mask is formed. An oxide etch to remove exposed oxide and a silicon etch to remove exposed silicon epitaxial layer are performed using the patterned body contact mask. The silicon etch can etch through the source regions, for example to a depth of between about 0.2 microns to about 0.4 microns, to result in the contact openings as depicted in FIG. 9. A body contact implant, for example a shallow BF_2 or boron implant, with an optional deeper boron implant to a dose of between about 5E14 atoms/cm^2 and about 4E15 atoms/cm^2, can form body contact regions 90A-90E. An optional anneal, for example using rapid thermal processing (RTP) at a temperature of between about 950°C to about 1,100°C or a diffusion can be performed.

[0033] After an optional thin oxide deposition, a trench-substrate-contact (TSC) mask 100 can be formed as depicted in FIG. 10. Mask 100 exposes the substrate in the region of body implant portion 70B, with the remainder of the depicted substrate protected by mask 100. Any exposed oxide is etched, then the epitaxial layer 46 and the semiconductor substrate 40 are etched to result in a structure similar to FIG. 11 having TSC contact opening 110. An optional trench bottom implant can be performed to enhance electrical conductivity with a subsequently formed conductive layer. Resist layer 100 can then be removed and an optional anneal can be performed to result in the structure similar to FIG. 12.

[0034] A thin oxide etch to pull back the oxide from the top horizontal surface of the source can be performed, then a thin conformal titanium (Ti) and titanium nitride (TiN) deposition can be performed to result in the conductive metal layer 130 as depicted in FIG. 13. A Ti layer between about 100 Å and about 500 Å, and a TiN layer between about 500 Å to about 1,500 Å would be sufficient.

[0035] An RTP metal anneal at a temperature of between about 600°C and about 800°C for a duration of 20 seconds to 60 seconds in an N_2 ambient can be performed to convert the titanium metal layer which contacts the silicon of the epitaxial layer and silicon substrate to titanium silicide ($TiSi_2$) and to densify the TiN to form the TSC metal. An optional tungsten (W) or tungsten silicide (WSi_x) deposition can be performed to further reduce the electrical resistance of the TSC structure and to optionally fill the deep trenches to result in the structure of FIG. 14 including metal layer 140. However, it should not be necessary to completely fill the trenches with conductor since the metal is sufficiently conductive and dielectrics will subsequently be deposited on exposed surfaces, which will fill the trenches to result in a sufficiently planar surface.

[0036] Next, a trench-metal mask 150 can be formed followed by a metal etch to result in the FIG. 15 structure. The metal etch can be performed until underlying dielectric is expose, with an additional over-etch to clear any remaining stringers. This forms individual conductive structures 152A-152E. Structures 152A, 152B will form gate shields to the high-side gate portions 66A, 66B, structure 152C will provide a portion of a floating guard ring, structures 152D and 152E will provide contact portions to the low-side VDMOS source. Thus these functions are performed using different parts of a single conductive structure, which can include one or more conductive layers.

[0037] Resist 150 can be stripped, then a low temperature oxide (LTO) can be deposited to a thickness of between about 300 Å and about 1,000 Å followed by a borophosphosilicate glass (BPSG) layer between about 3,000 Å to about 9,000 Å to result in oxide layer 160 as depicted in FIG. 16. The oxide can be flowed and densified at a temperature between about 800°C to about 900°C.

[0038] A contact mask can be formed over the oxide 160, then an oxide etch to remove exposed oxide portions can be performed. An N+ implant of arsenic or phosphorous to a dose of between about 1E14 atoms/cm^2 to about 6E16 atoms/cm^2 at an energy of between about 20 KeV to about 80 KeV with 0° tilt would result in the structure similar to FIG. 17. The implant can be diffused using an RTP process at a temperature of between about 850°C to about 900°C for about 60 seconds using an N_2 gas flow. The N+ implant forms an N+ drain 170 of the high side LDMOS device and an N+ gate contact to the low-side gate. Also exposed during the etch of oxide layer 160 using the contact mask are low-side transistor source metal 174, 176.

[0039] Subsequently, a Ti/TiN deposition of barrier metal 180, an RTP anneal, a deposition of tungsten 182, and a tungsten etch back can be performed to result in tungsten contact plugs 182A-182D. A deposition and patterning of a conductor such as aluminum copper (AlCu) can form metal structures 184A-184C. Structure 184A can form a conductive drain interconnect and be electrically coupled with voltage in (V_{IN}) to provide a high-side transistor drain interconnect. Structure 184B can form a conductive source interconnect and be electrically coupled with ground to provide a low-side transistor source interconnect. Structure 184C provides a gate contact to the low-side transistor gate. Thus these functions are performed using different parts of a single conductive structure, which can include one or more conductive layers.

[0040] Additionally, body region 70C can provide an integrated floating guard ring to increase trench-DMOS body-drain breakdown voltage. This structure is formed using processing step which also form high-side LDMOS transistor and low-side VDMOS transistor structures.

[0041] The method can result in formation of a high-side output power device including an LDMOS transistor device having a planar gate and a low-side VDMOS device having a trench-gate. The same conductive (polysilicon) layer can be used for the gate of each device, and the same body implant can form a body region for each device within the epitaxial layer. Additionally, the substrate provides the switched node (i.e. output node) for the device.

[0042] As depicted in FIG. 18, a first portion 152A of metal TSC layer 140 is interposed between gate structure 66A and high-side LDMOS drain metal 184A, and a second portion 152B is interposed between gate structure 66B and drain metal 184A. The structures 152A, 152B, tied to the substrate 50 through the TSC contacts, provide gate shields which can minimize parasitic capacitance and reduce or eliminate parasitic source inductance. The shield function can shield the gate from the electric field surrounding the overlying conductive drain interconnect to reduce gate-to-drain capacitance (C_{GD}), and minimize the gate and gate-drain charges (Q_G).

[0043] An embodiment of the invention also provides a device having a body contact on all sides of the TSC structure, for example as depicted in FIG. 19. This can result from the formation of the TSC 152B (and analogous structure 152A) inside the body contact region 90B, which exposes the top of the body contact at the entire periphery of the TSC. Therefore, the TSC can be laid out in stripes while maintaining a low resistance body contact.

[0044] An embodiment of the device includes nine patterned mask steps, which include an active area mask, a deep body mask, a gate trench mask, a gate polysilicon mask, a body contact mask, a TSC mask, a trench metal mask, a contact mask, and a metal mask. Various cross sections depict an n-channel LDMOS high-side transistor with its drain terminated by the TSC, and with enhanced deep body contact. Also depicted is an n-channel trench-gate DMOS low-side device with a floating P-body guard ring as body edge termination and patterned gate connection.

[0045] Another embodiment is depicted in FIG. 20. This embodiment includes an integrated Schottky diode which can result in different electrical characteristics from the embodiment depicted in FIG. 18, for example. The Schottky diode is provided by metal structure 190 in contact with n-type epitaxial region 192. The contact to the low-side VDMOS gate (analogous to structures 182D and 184C in FIG. 18) is located at a different cross section of the device. This structure can be implemented without any additional mask steps by using a region of the field oxide to block the body implant. In another embodiment, a body mask can be used to block the body implant from the Schottky contact region, and a source mask to block the source implant from the same Schottky contact region. The source contact for the low-side VDMOS device would require slightly more space than with the previous embodiment. To simplify explanation, additional processing details will not be discussed herein, with a slight modification of the process detailed in FIGS. 2-18 providing a device similar to that depicted in FIG. 20.

[0046] Thus an embodiment of the invention has a low implementation cost (low die cost), results in a die which has low parasitic inductance and capacitance, has a minimum die size, and can be optimized based on the circuit requirements. An embodiment can include the use of a high side and low side device on a single die such that the output is available on the back side of the die. A single die can be used for both high-side and low-side power devices fabricated using an efficient process flow with minimal processing steps. The device can be configured to minimize or eliminate any parasitic inductance. The resulting device is compatible with structures which feature high-frequency of operation and minimized parasitic capacitances. At least partly because of a minimum number of components, the assembly cost is minimized. The device is capable of achieving higher power densities than some other devices.

[0047] In operation, the heavily doped substrate is the switched node. Thus the back side of the wafer is also the switched node (output) of the output stage, and can therefore be electrically coupled with devices requiring connection to the output stage. Assuming N-channel device are used for both the high-side and low-side power devices, no parasitic inductance between the switched node and the source of the high-side device may be possible, as well as to the drain of the low-side device.

[0048] Further, a single layer of metal is required to interconnect each of the drain of the high-side device, the source of the low-side device, and the gates of the two devices.

[0049] Additionally, a trench-substrate-contact structure connecting to the semiconductor substrate of the device can function as a high-side device gate shield structure to minimize parasitic capacitance and protect the gate from electrical influences from other device structures, for example from an overlying drain interconnect in addition to eliminating the parasitic source inductance.

[0050] In various embodiments, the device structures are formed using a process which combines the TSC structure with a gate shield, which eliminates a number of processing stages.

[0051] Forming the high-side output power device and the low-side output power device on a single chip allows for a smaller area than forming the two devices on two separate chips. The device provides highly efficient operation and high-frequency through reduction or elimination of the parasitic inductance. Various embodiments enable the use of an efficient high-side structure (LDMOS) and an efficient low-side structure (trench-gate VDMOS with low R_{SP} on a single chip. The structure further provides an independent threshold voltage control even though the same body diffusion is used.

[0052] A chip including the output stage can be co-packaged with a controller IC to yield various benefits. For example, multiple products simply by changing the monolithic power die. Multiple products can leverage a single power-IC design. Because the output devices are formed on a die separate from the controller circuitry, the device provides reduced noise feedback to the controller, and reduced thermal feedback to the controller.

[0053] For most effective device operation in any power MOSFETs, low resistance contact connections between the source regions and body regions are needed. Low resistance contacts avoid having the parasitic bipolar transistor (NPN for an N-channel MOSFET) turn on (activate). If the parasitic bipolar turns on, device damage can occur, for example resulting from current run-away, etc. In an embodiment of the invention, the device body and source are integrated into one contact, with the source on a trench sidewall and the body contact at the trench bottom, with the conductive (metal) contact electrically coupled with both. The metal contact (the TSC contact) inside the trench connects all of these diffusion regions together in a very small area with low resistance.

[0054] Notwithstanding that the numerical ranges and parameters setting forth the broad scope of the invention are approximations, the numerical values set forth in the specific examples are reported as precisely as possible. Any numerical value, however, inherently contains certain errors necessarily resulting from the standard deviation found in their respective testing measurements. Moreover, all ranges disclosed herein are to be understood to encompass any and all sub-ranges subsumed therein. For example, a range of "less than 10" can include any and all sub-ranges between (and including) the minimum value of zero and the maximum value of 10, that is, any and all sub-ranges having a minimum value of equal to or greater than zero and a maximum value of equal to or less than 10, e.g., 1 to 5. In certain cases, the numerical values as stated for the parameter can take on negative values. In this case, the example value of range stated as "less that 10" can assume negative values, e.g. – 1, -2, -3, -10, -20, -30, etc.

[0055] While the invention has been illustrated with respect to one or more implementations, alterations and/or modifications can be made to the illustrated examples without departing from the spirit and scope of the appended claims. In addition, while a particular feature of the invention may have been disclosed with respect to only one of several implementations, such feature may be combined with one or more other features of the other implementations as may be desired and advantageous for any given or particular function. Furthermore, to the extent that the terms "including," "includes," "having," "has," "with," or variants thereof are used in either the detailed description and the claims, such terms are intended to be inclusive in a manner similar to the term "including." The term "at least one of" is used to mean one or more of the listed items can be selected. Further, in the discussion and claims herein, the term "on" used with respect to two materials, one "on" the other, means at least some contact between the materials, while "over" means the materials are in proximity, but possibly with one or more additional intervening materials such that contact is possible but not required. Neither "on" nor "over" implies any directionality as used herein. The term "conformal" describes a coating material in which angles of the underlying material are preserved by the conformal material. The term "about" indicates that the value listed may be somewhat altered, as long as the alteration does not result in nonconformance of the process or structure to the illustrated embodiment. Finally, "exemplary" indicates the description is used as an example, rather than implying that it is an ideal. Other embodiments of the invention will be apparent to those skilled in the art from consideration of the specification and practice of the invention disclosed herein. It is intended that the specification and examples be considered as exemplary only, with a true scope and spirit of the invention being indicated by the following claims.

Claims:

1. A method for forming a semiconductor device, the method comprising:

forming, on a semiconductor die, a high-side transistor comprising a lateral diffusion metal oxide semiconductor (LDMOS) device;

forming, on the semiconductor die, a low-side transistor comprising a trench-gate vertical diffusion metal oxide semiconductor (VDMOS) device;

forming, on the semiconductor die, a single conductive structure which forms a portion of a gate of the high-side transistor and a portion of a gate of the low-side transistor; and

performing an unmasked blanket body implant in a layer of the high-side transistor and a layer of the low-side transistor to form high-side and low-side body regions.

2. The method of claim 1 wherein the single conductive structure is a first single conductive structure and the method further comprises:

etching a layer comprising a conductor to form a contact to the semiconductor wafer section, a shield for the portion of the gate of the high-side transistor, a contact to a floating guard ring to the trench-gate VDMOS transistor, and a contact to a source of the trench-gate VDMOS transistor from a second single conductive structure.

3. The method of claim 2, further comprising etching a layer comprising a conductor to form a drain contact to a drain of the high-side LDMOS transistor, a source contact to a source of the trench-gate low-side VDMOS transistor, a gate contact to the

gate of the trench-gate low-side VDMOS device, and a gate contact to the gate of the high-side transistor from a third single conductive structure.

4. The method of claim 1, further comprising forming a conductive trench-source-contact structure which electrically shorts a gate shield for the high-side LDMOS transistor gate to the substrate, which contacts the semiconductor substrate, and which contacts a body contact on all sides of a portion of the trench-source-contact structure.

5. The method of claim 1 wherein the single conductive structure is a first single conductive structure and the method further comprises forming a second single conductive structure which forms:

a contact to a source region of the high-side transistor;

a contact to a body region of the high-side transistor;

a contact to a source region of the low-side transistor;

a contact to a body region of the low-side transistor;

a gate shield for a transistor gate of the high-side transistor;

an electrical connection between the source and body of the high-side device; and

an electrical connection between a drain of the low-side device and a semiconductor substrate of the semiconductor die.

6. The method of claim 1, wherein the semiconductor die is a first semiconductor die and the method further comprises:

providing a second semiconductor die different from the first semiconductor die comprising voltage converter controller circuitry; and

electrically coupling the voltage converter controller circuitry with the first semiconductor die.

7. The method of claim 6, further comprising co-packaging the first semiconductor die and the second semiconductor die into a single semiconductor device.

8. The method of claim 1 wherein the single conductive structure is a first single conductive structure and the method further comprises:

forming a conductive trench contact having at least a portion within a trench in a semiconductor substrate;

forming at least one conductive gate portion of the LDMOS device; and

forming a gate shield interposed between the at least one conductive gate portion of the LDMOS device and a structure which overlies the gate shield,

wherein the gate shield and the conductive trench contact are formed from a second single conductive structure.

9. The method of claim 8 further comprising etching a layer comprising a conductor to define:

a conductive drain interconnect electrically coupled to a drain of the LDMOS device; and a conductive source interconnect electrically coupled to a source of the VDMOS device,

wherein the conductive drain interconnect and the conductive source interconnect are formed from a third single conductive structure.

10. The method of claim 9, further comprising:

electrically coupling a portion of the third single conductive structure which forms the conductive drain interconnect to voltage in (VIN); and

electrically coupling a portion of the third single conductive structure which forms the conductive source interconnect to ground.

11. The method of claim 1 further comprising forming a conductive contact within a trench to electrically couple a high-side transistor source and a high-side transistor body.

12. A method of forming a semiconductor device, the method comprising:

forming a high-side transistor comprising a lateral diffusion metal oxide semiconductor (LDMOS) device on a single semiconductor die;

forming a low-side transistor comprising a trench-gate vertical diffusion metal oxide semiconductor (VDMOS) device on the single semiconductor die; and

forming a single conductive structure which forms a portion of a gate of the high-side transistor and a portion of a gate of the low-side transistor;

wherein forming the high-side transistor comprises:

forming a body region;

forming a body contact region in the body region; and

forming a trench-substrate-contact (TSC) through the body contact region and the body region such that the TSC contacts a top surface of the body contact region and a side of the body contact region.

13. The method of claim 12 wherein the single conductive structure is a first single conductive structure and the method further comprises:

forming a second single conductive structure which forms a contact to the semiconductor wafer section, a shield for the portion of the gate of the high-side transistor, a contact to a floating guard ring to the trench-gate VDMOS transistor, and a contact to a source of the trench-gate VDMOS transistor.

14. The method of claim 13, further comprising:

forming a third single conductive structure which forms a drain contact to a drain of the high-side LDMOS transistor, a source contact to a source of the trench-gate low-side VDMOS transistor, and a gate contact to the trench-gate low-side VDMOS device gate.

15. The method of claim 12, wherein forming the TSC comprises forming the TSC such that the TSC electrically shorts a gate shield for the high-side transistor to the substrate, the TSC contacting the semiconductor substrate and the body contact region on all sides of a portion of the TSC.

16. The method of claim 12, wherein the single semiconductor die is a first semiconductor die and the method further comprising:

forming a second semiconductor die different from the first semiconductor die comprising voltage converter controller circuitry electrically coupled with the first semiconductor die.

17. The method of claim 16, further comprising co-packaging the first semiconductor die and the second semiconductor die into a single semiconductor device.

18. The method of claim 12 wherein the single conductive structure is a first single conductive structure, and the method further comprises:

forming a conductive trench contact having at least a portion within a trench within a semiconductor substrate;

forming at least one conductive gate portion of the LDMOS device; and

forming a gate shield interposed between the at least one conductive gate portion of the LDMOS device and a structure which overlies the gate shield,

wherein the gate shield and the conductive trench contact are a second single conductive structure.

19. The method of claim 18 further comprising:

forming a conductive drain interconnect electrically coupled to a drain of the LDMOS device; and forming a conductive source interconnect electrically coupled to a source of the VDMOS device,

wherein the conductive drain interconnect and the conductive source interconnect are a third single conductive structure.

20. The method of claim 19, further comprising:

electrically coupling the conductive drain interconnect to voltage in (VIN); and

electrically coupling the conductive source interconnect to ground.

ABSTRACT OF THE DISCLOSURE

A voltage converter includes an output circuit having a high-side device and a low-side device which can be formed on a single die (a "PowerDie"). The high-side device can include a lateral diffused metal oxide semiconductor (LDMOS) while the low-side device can include a trench-gate vertical diffused metal oxide semiconductor (VDMOS). The voltage converter can further include a controller circuit on a different die which can be electrically coupled to, and co-packaged with the output circuit.